Introducing: The Calibre nm Platform and Calibre nmDRC

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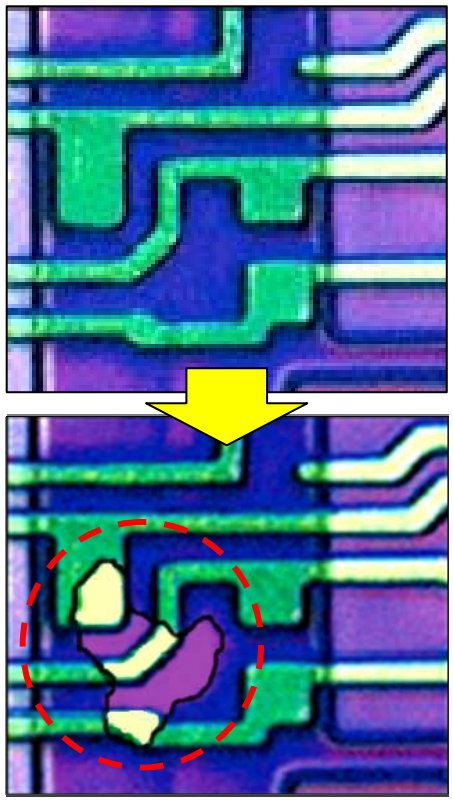
VP and GM, Design to Silicon Division

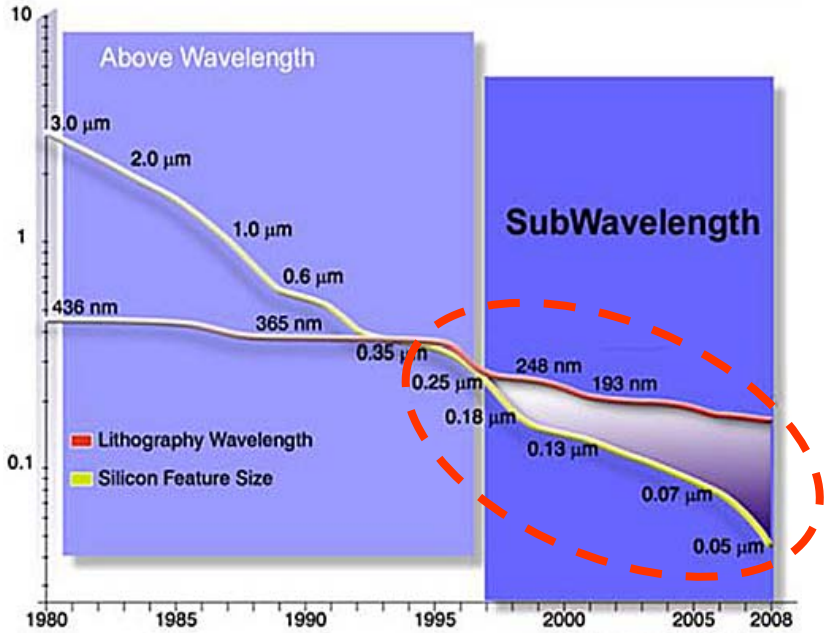
June/July 2006

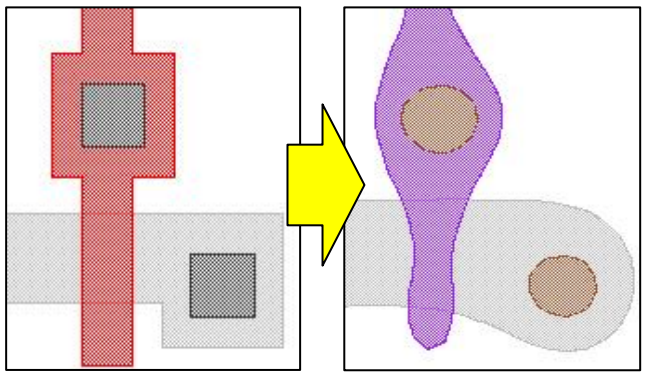
Mentor Graphics®

Yield Issues in Nanometer Technologies

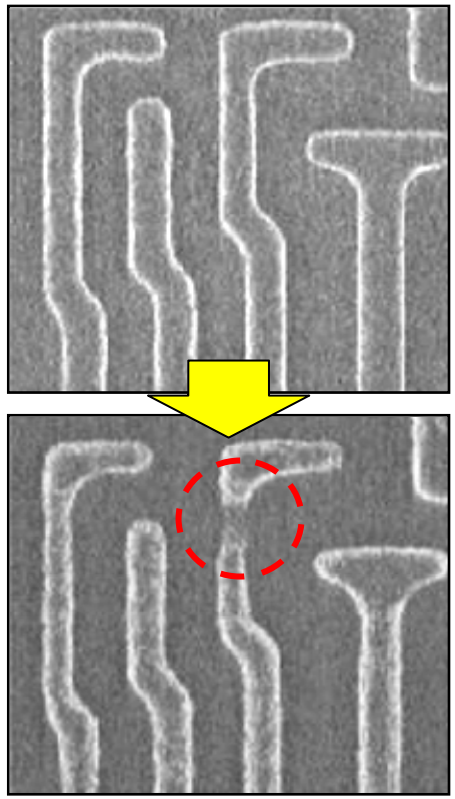


Random





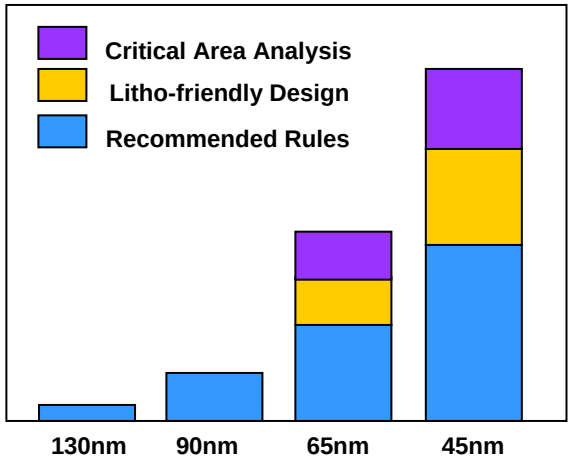
Parametric



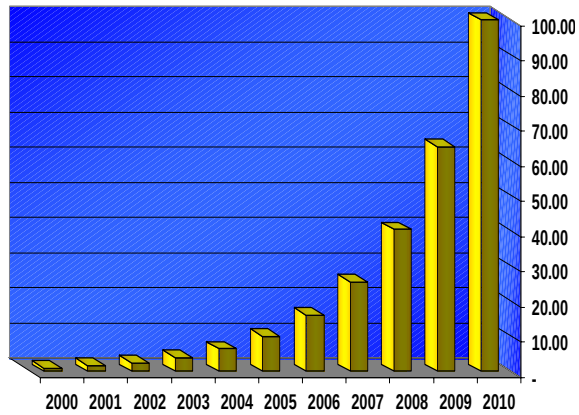
Systematic

The Wonderful and Frightening World of Physical Verification and DFM

Additional DFM Rules

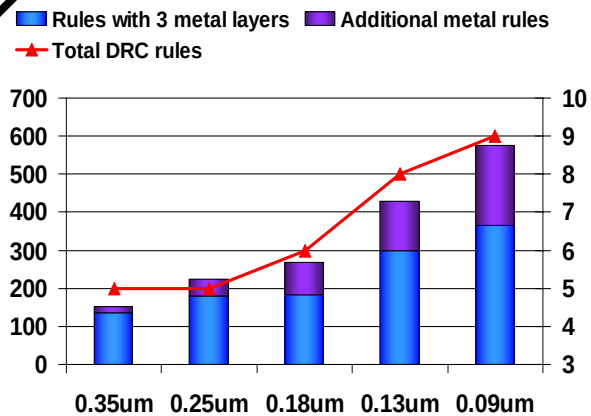


Total Geometric Shape Count

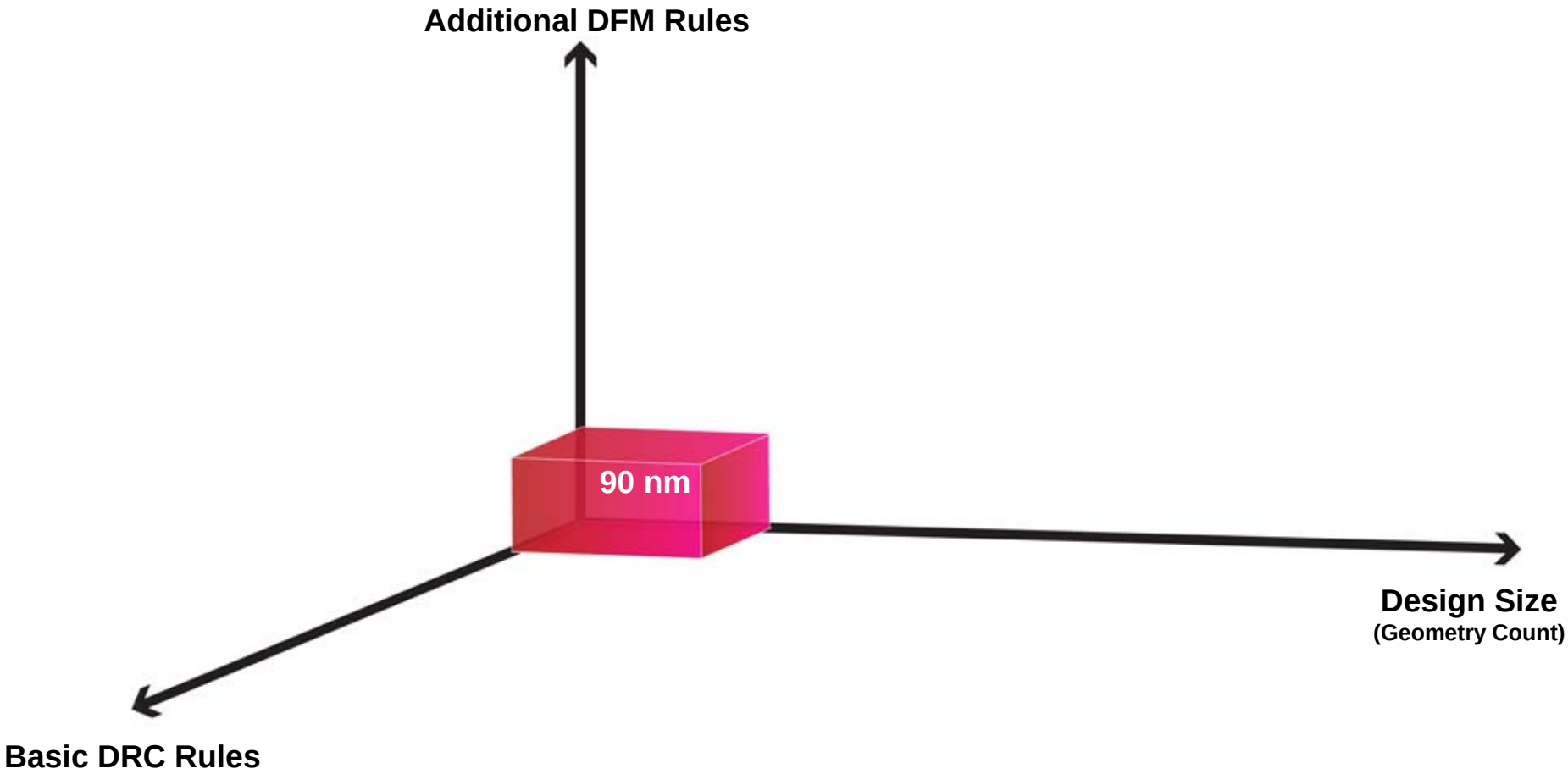


Design Size (Geometry Count)

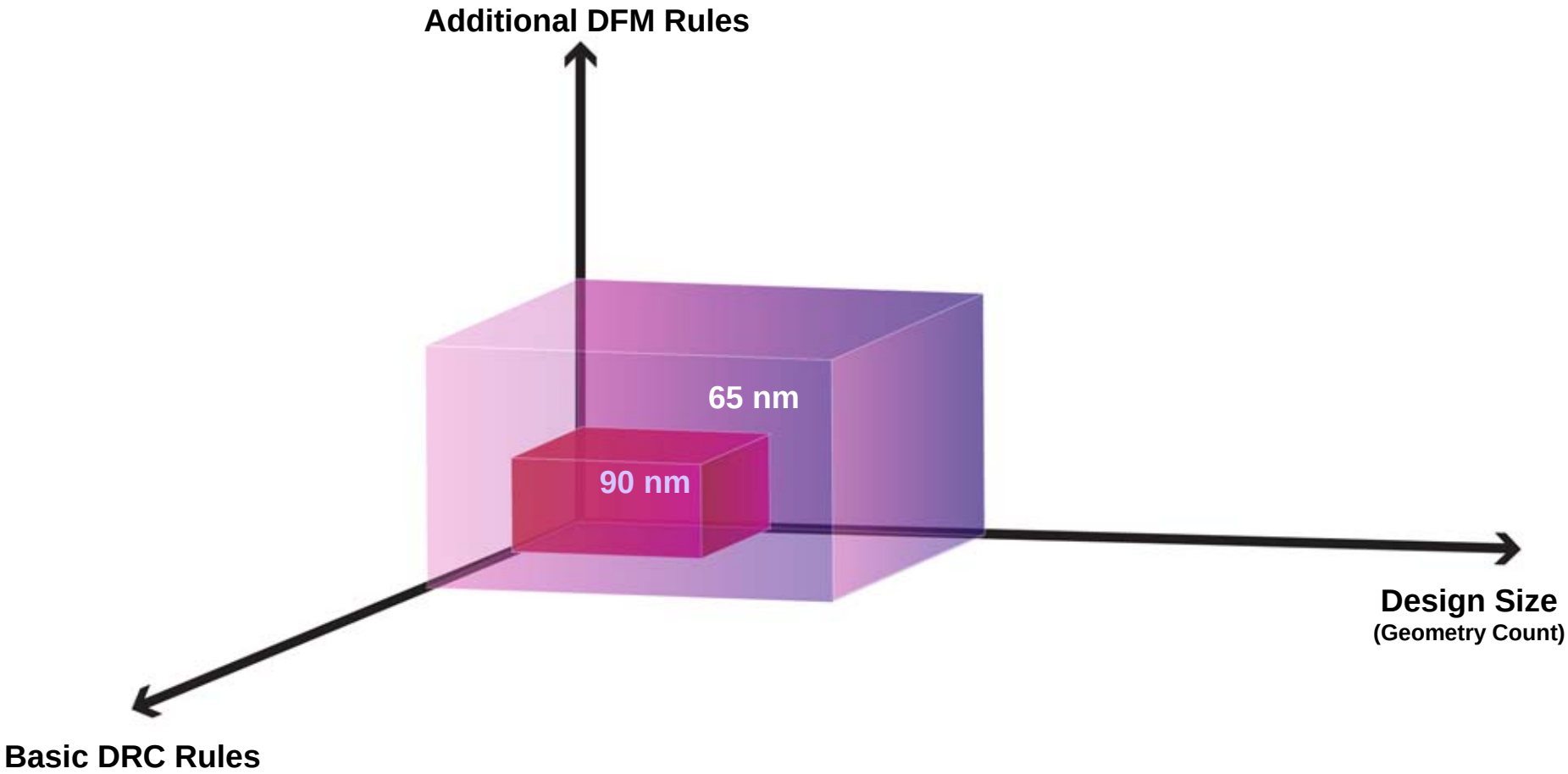
Basic DRC Rules



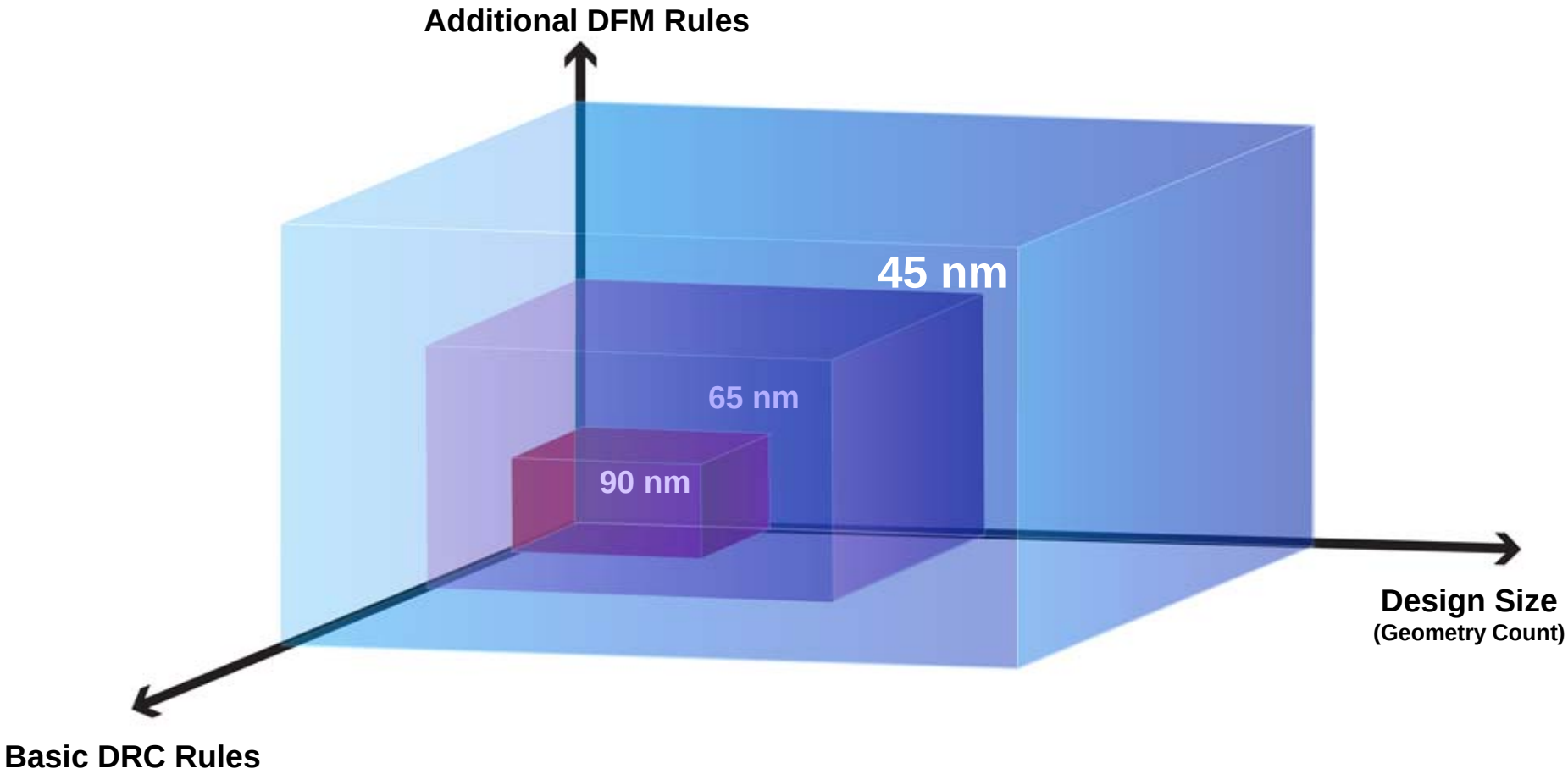
Computational Complexity



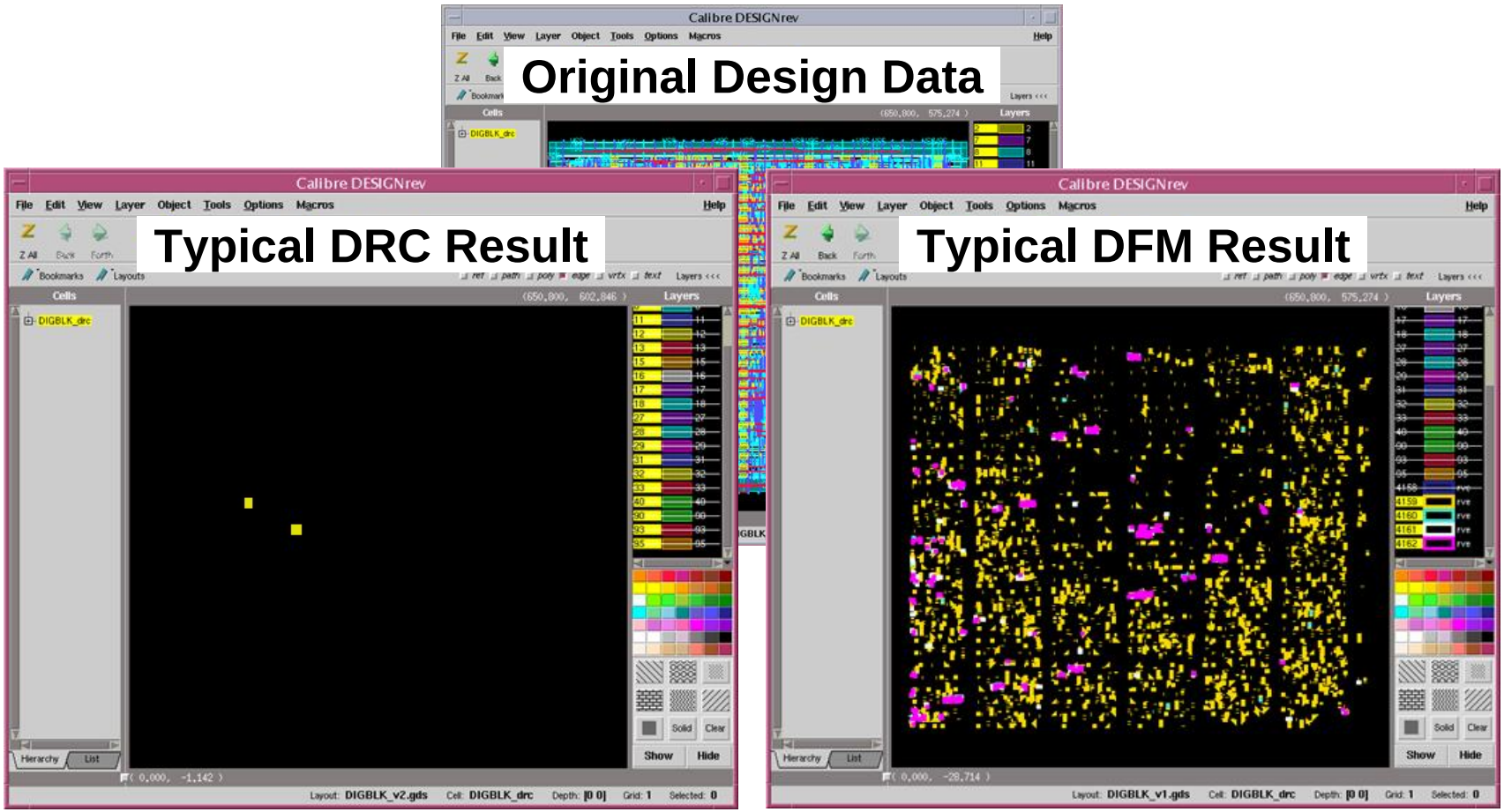
Computational Complexity



Computational Complexity

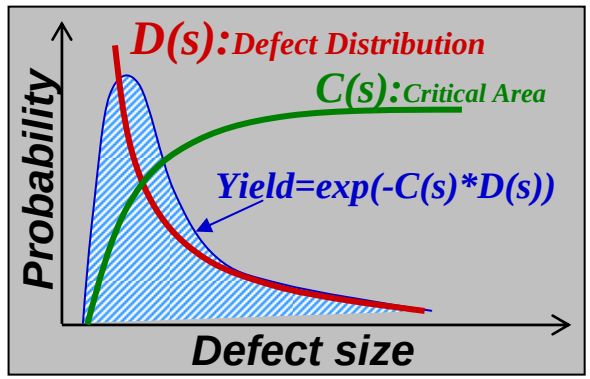


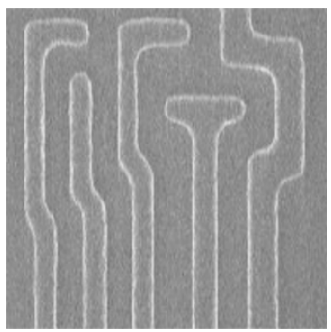
Design: Seeing through the Fog

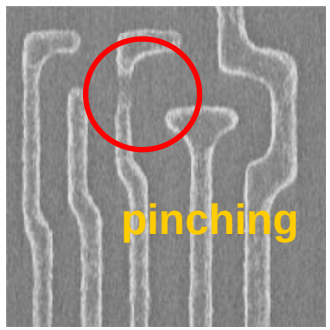


Complexity Drives a Change From Rules to Models

- **Major DFM capabilities are moving from a rules-based approach to a models-based approach**
  - **Critical Area Analysis (CAA)**
  - **Litho-friendly Design (LFD)**

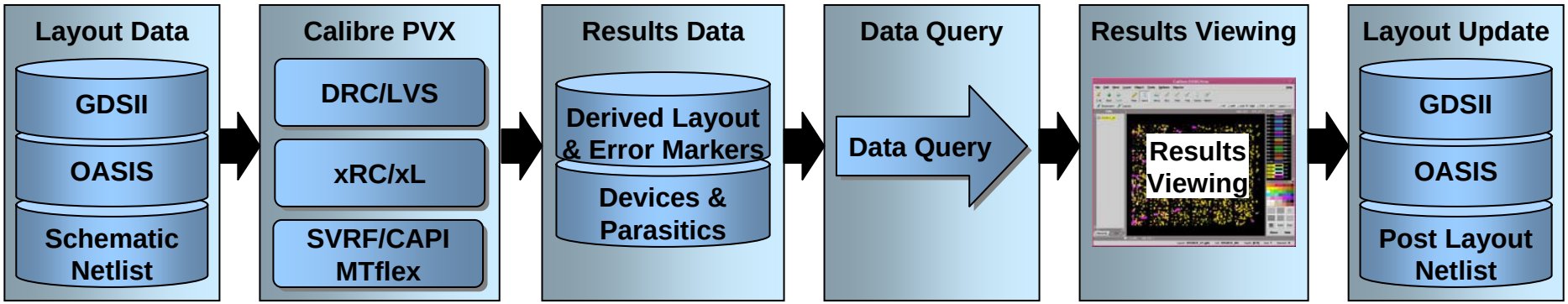




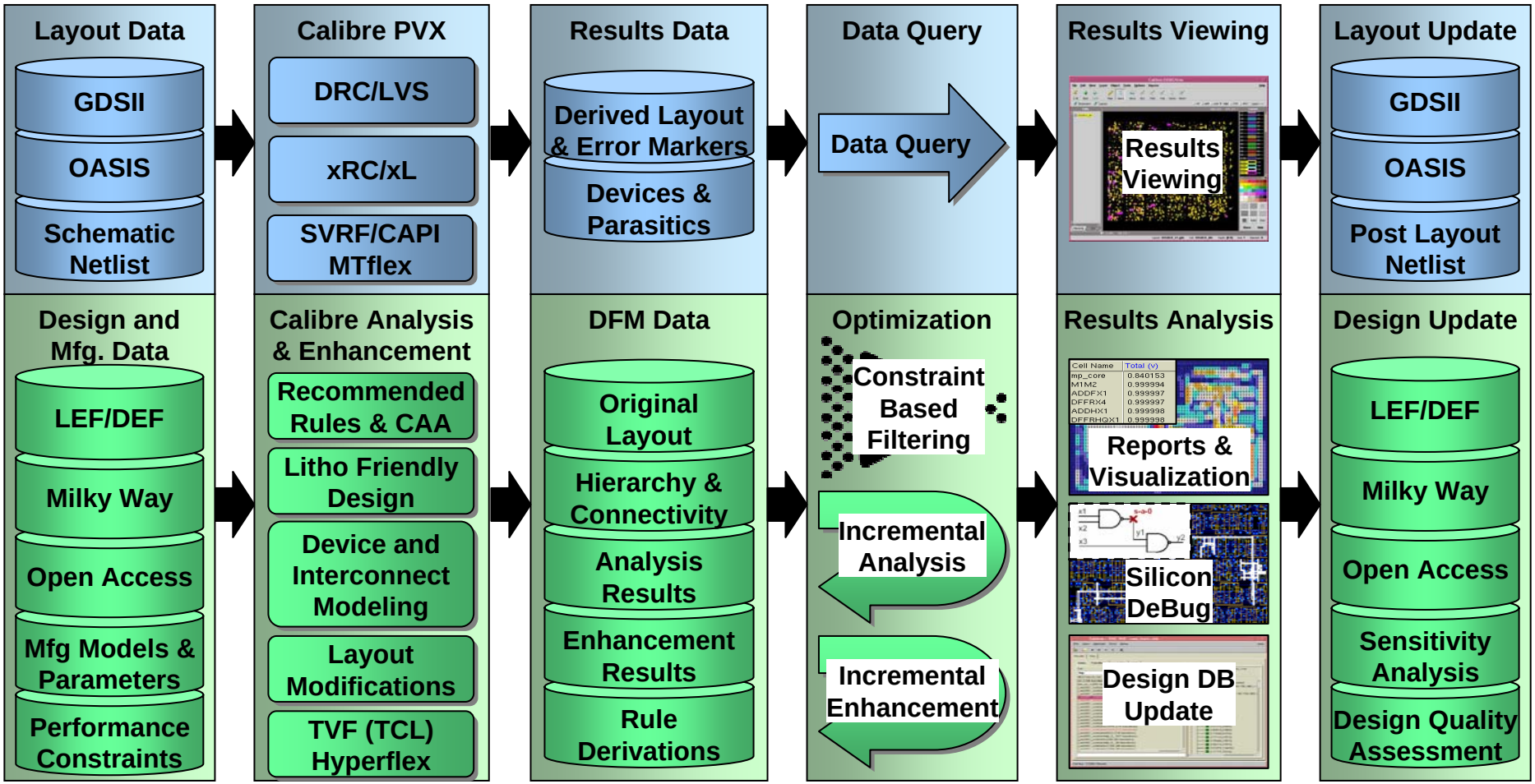


Increasing complexity and the rise in multiple issues will force this trend to continue.

Yesterday's Calibre Platform

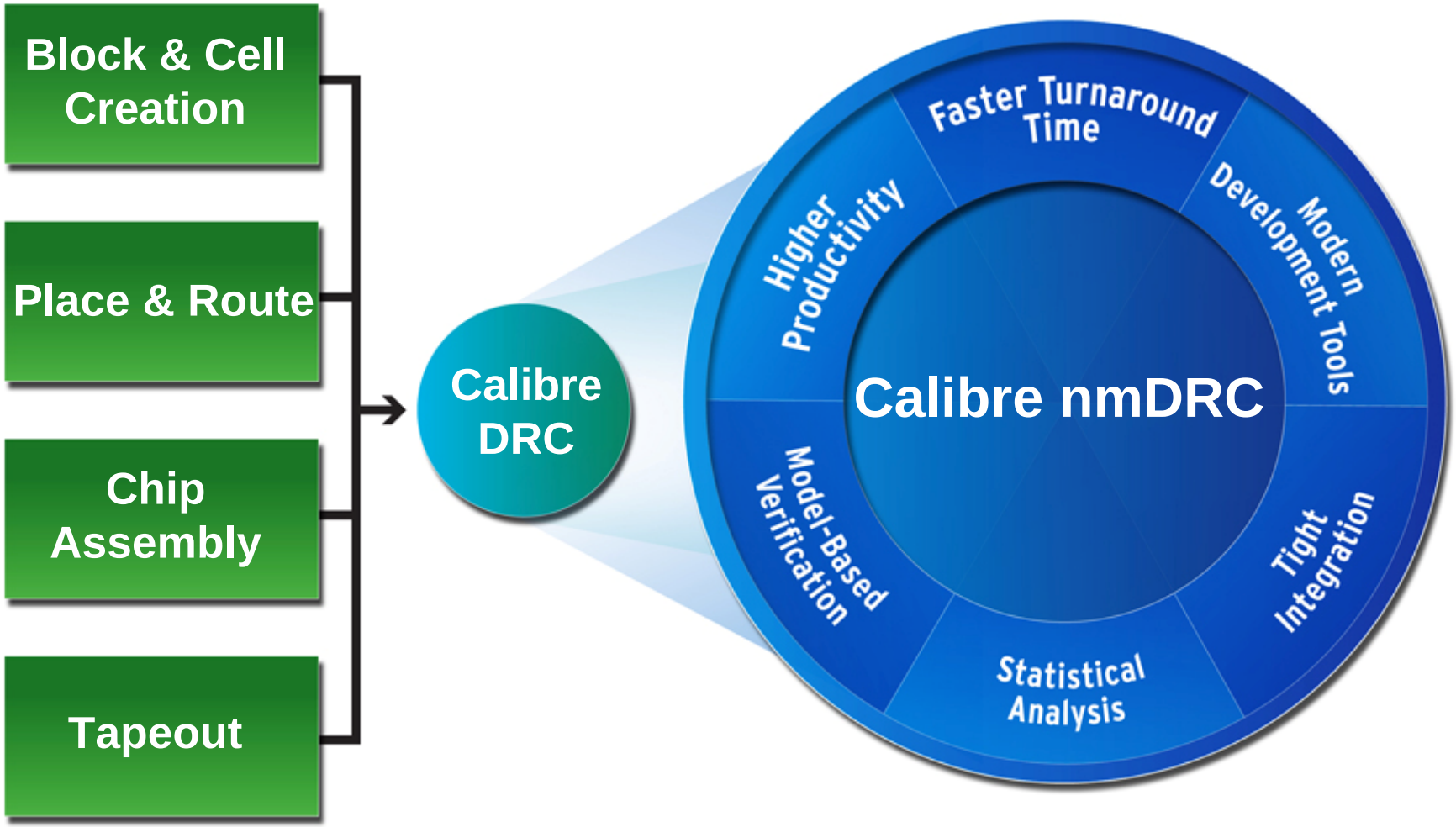


The New Calibre nm Platform

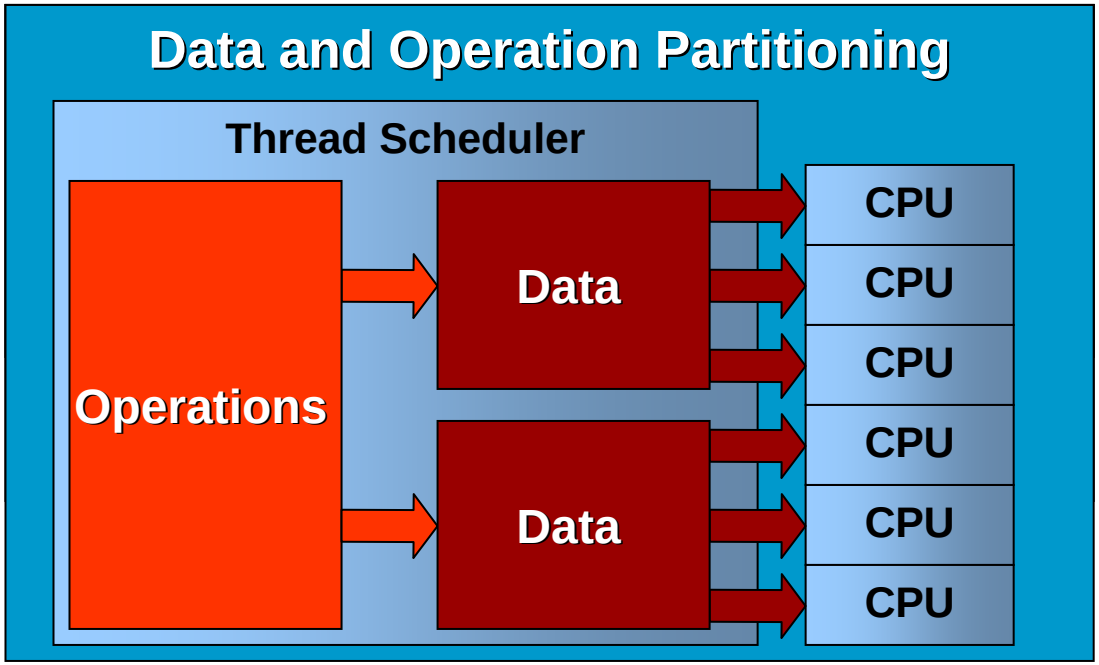


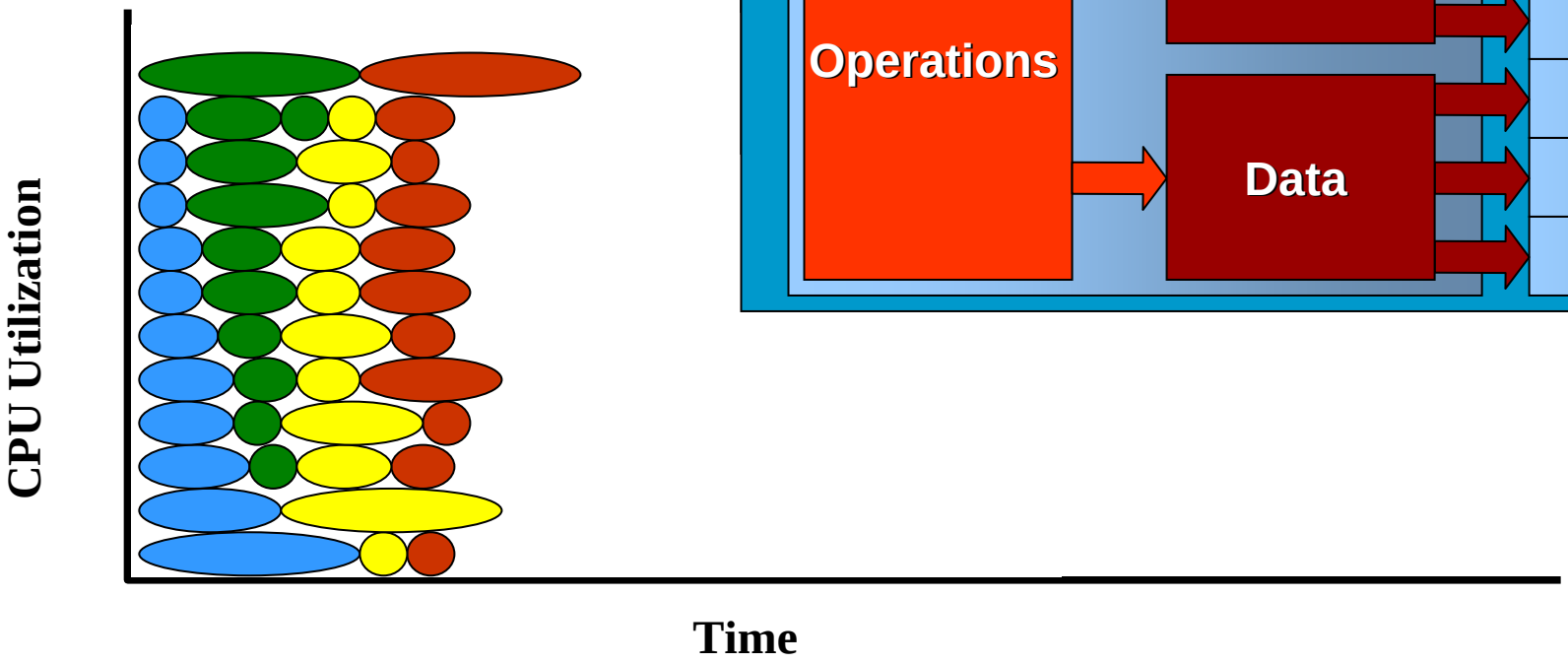
Calibre nm Platform

Introducing Calibre nmDRC

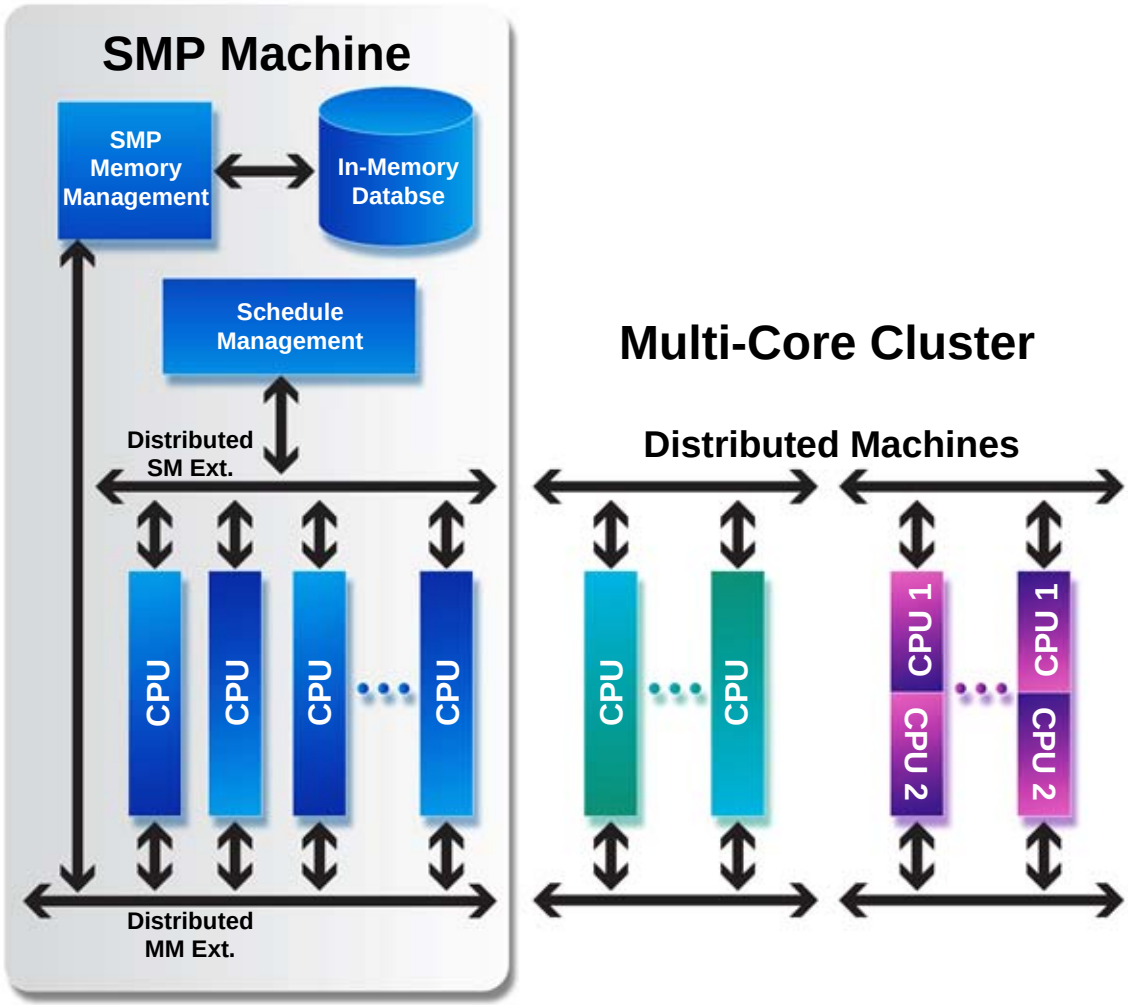


Achieving Faster Turn Around Times (TAT)





Multiprocessing Environment



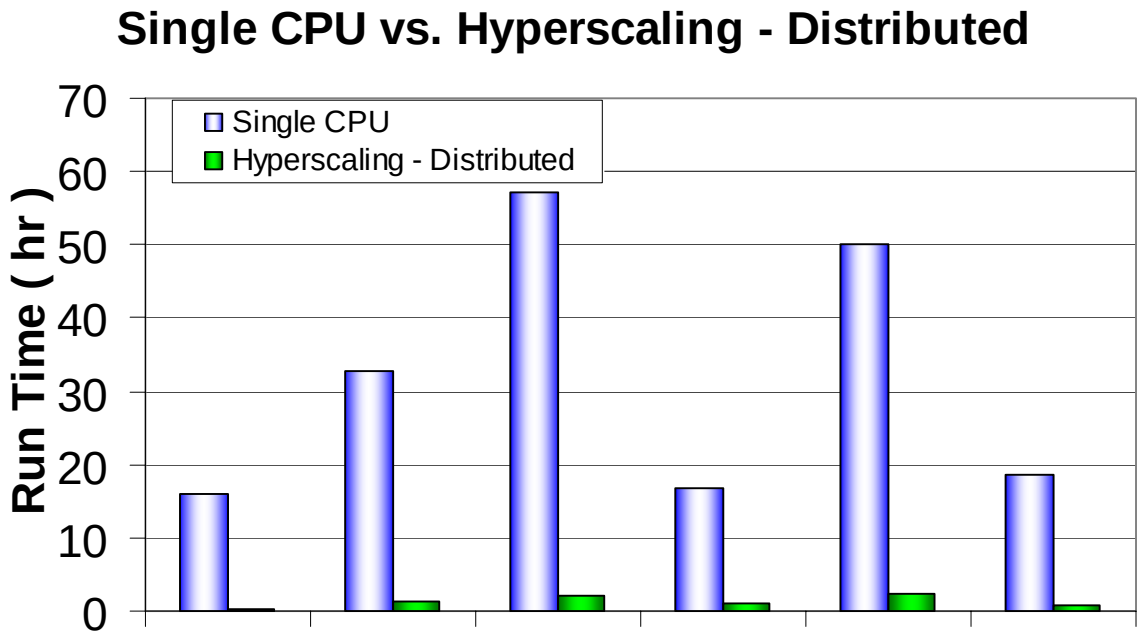
Single CPU

SMP

Multi-Core Cluster

Calibre nmDRC
Performance Improvement

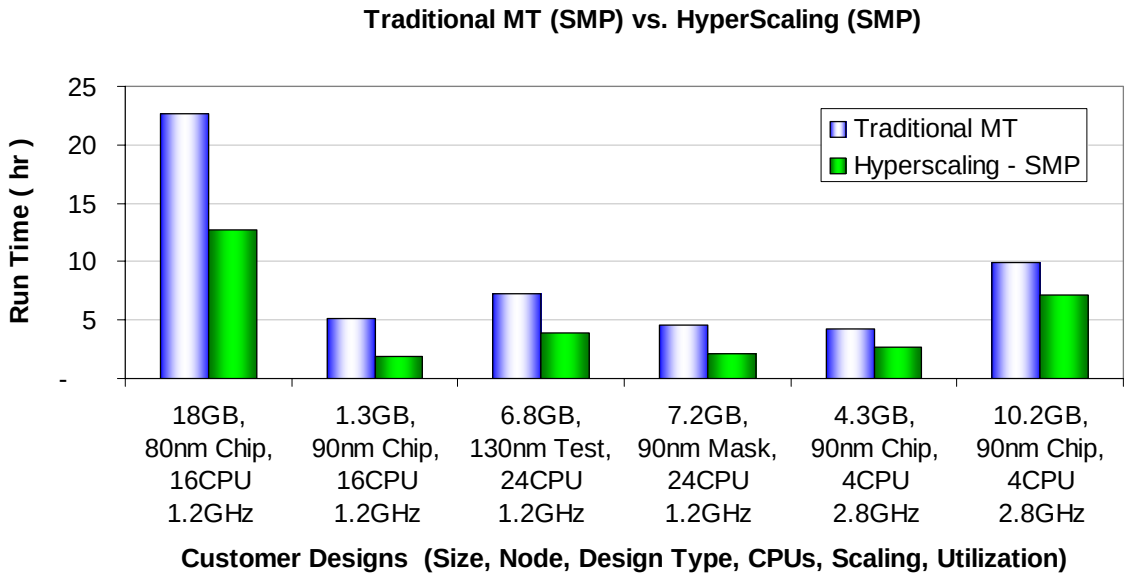
- **Hyperscaling provides a dramatic speed up**
- **Excellent scaling over a range of job sizes and types**



Customer	A	B	C	D	E	F
DB Size, Design Node	0.5GB, 90nm	6.8GB, 130nm	7GB	7.2GB, 90nm	11GB, 90nm	1.3GB, 90nm
CPU's	40	40	32	24	32	40
Run Time	0:18	1:19	2:01	1:00	2:18	0:48

Calibre nmDRC
Performance Improvement - SMP

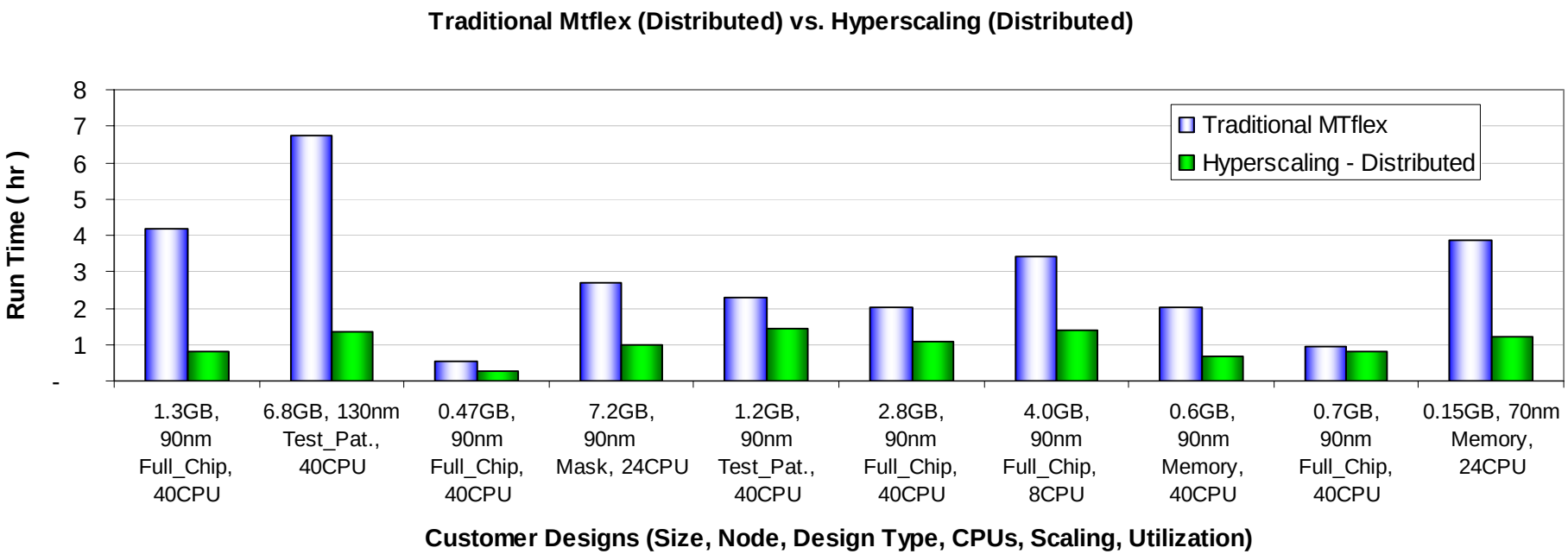
- **Hyperscaling delivers improved TAT on existing CAPEX**
  - **Extends life**
  - **Supports a wide range of H/W platforms**
  - **Does not *require* H/W investment**



- **Average improvement 1.9x**

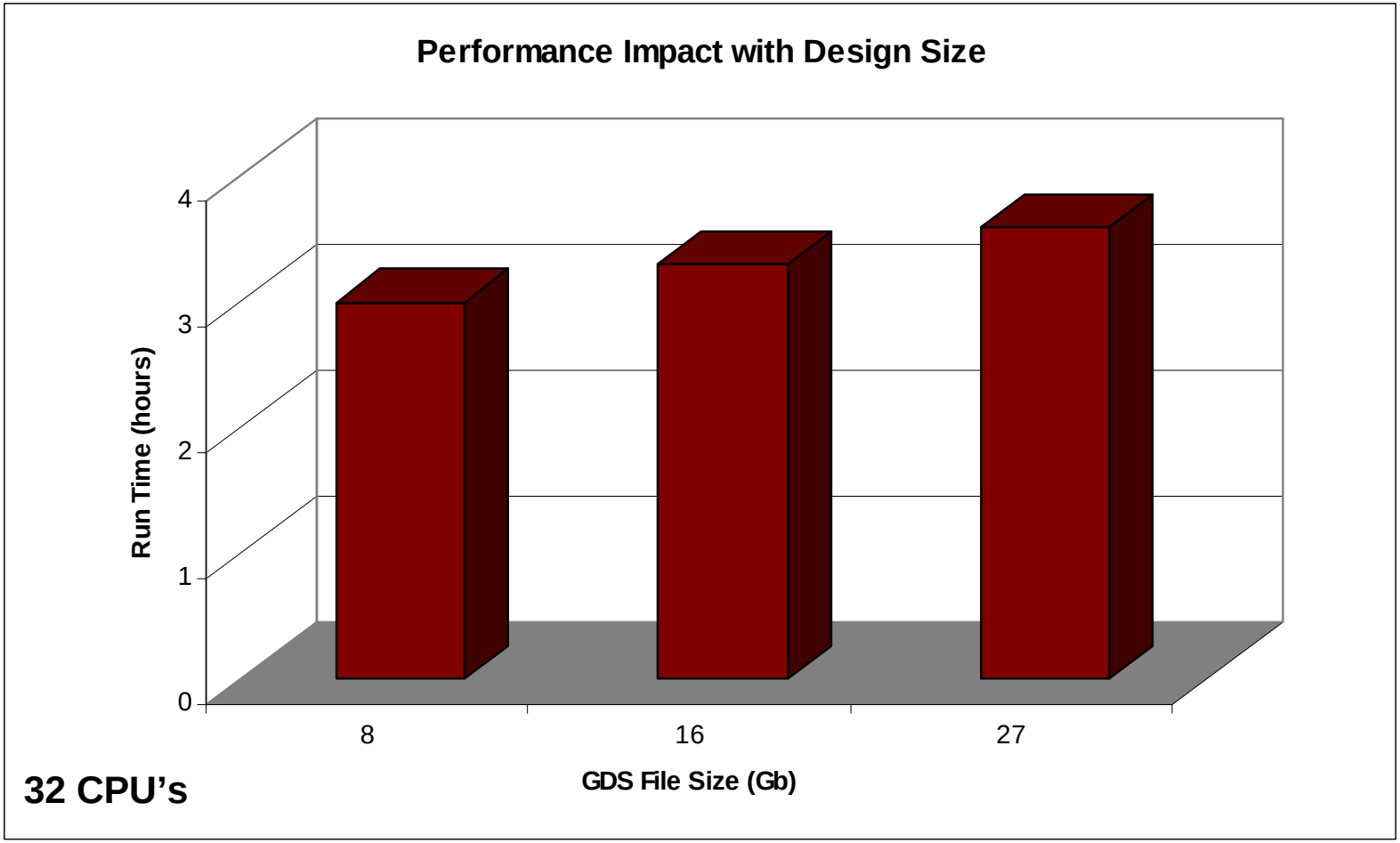
Calibre nmDRC
Performance Improvement - Distributed

- **Hyperscaling provides fast TAT on distributed hardware**



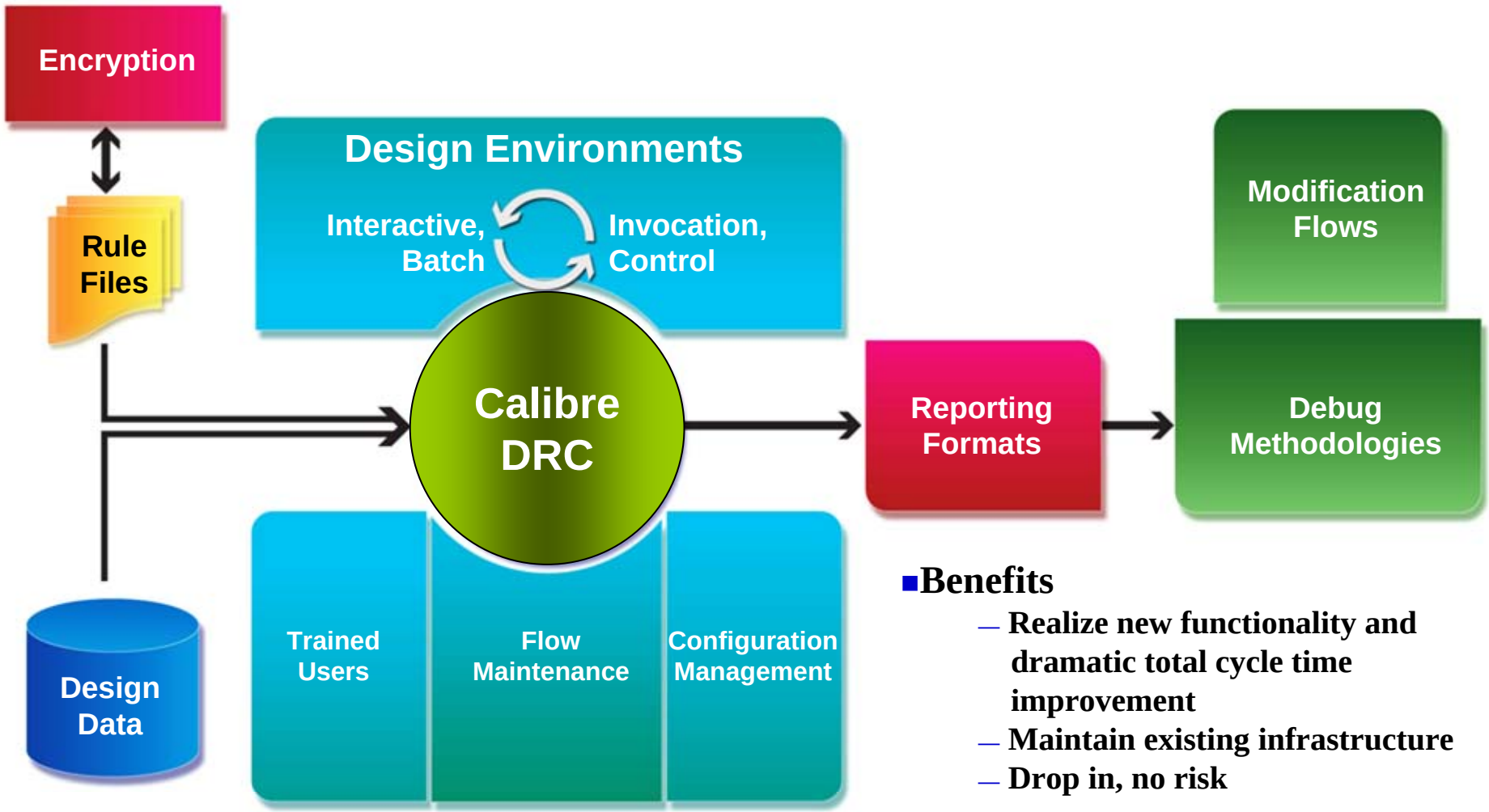
- **Average improvement 2.9x**
- **4 longest designs improved by 3.8x**

Performance Scaling with Design Size



Performance insensitive to data volume

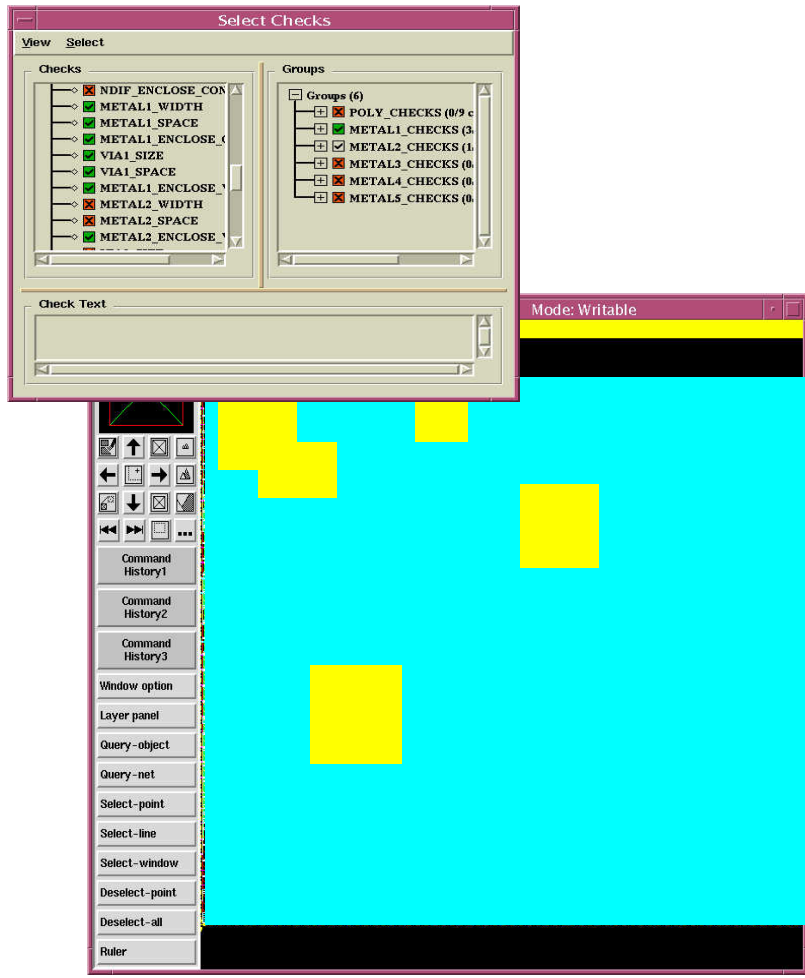
Calibre nmDRC: Drops Into Current CAD Environment Without Disruption



- **Benefits**
  - Realize new functionality and dramatic total cycle time improvement
  - Maintain existing infrastructure
  - Drop in, no risk

Calibre nmDRC
Dramatically Reduced Iteration Runtimes

- **Incremental DRC**
  - **Highlight errors as identified**
    - **Begin debug immediately - before job completion**
  - **Automatically identify changed regions**
    - **DB Diff**
  - **Minimize subsequent runtimes**
    - **Stream-out only changed areas**
    - **Run only affected checks**

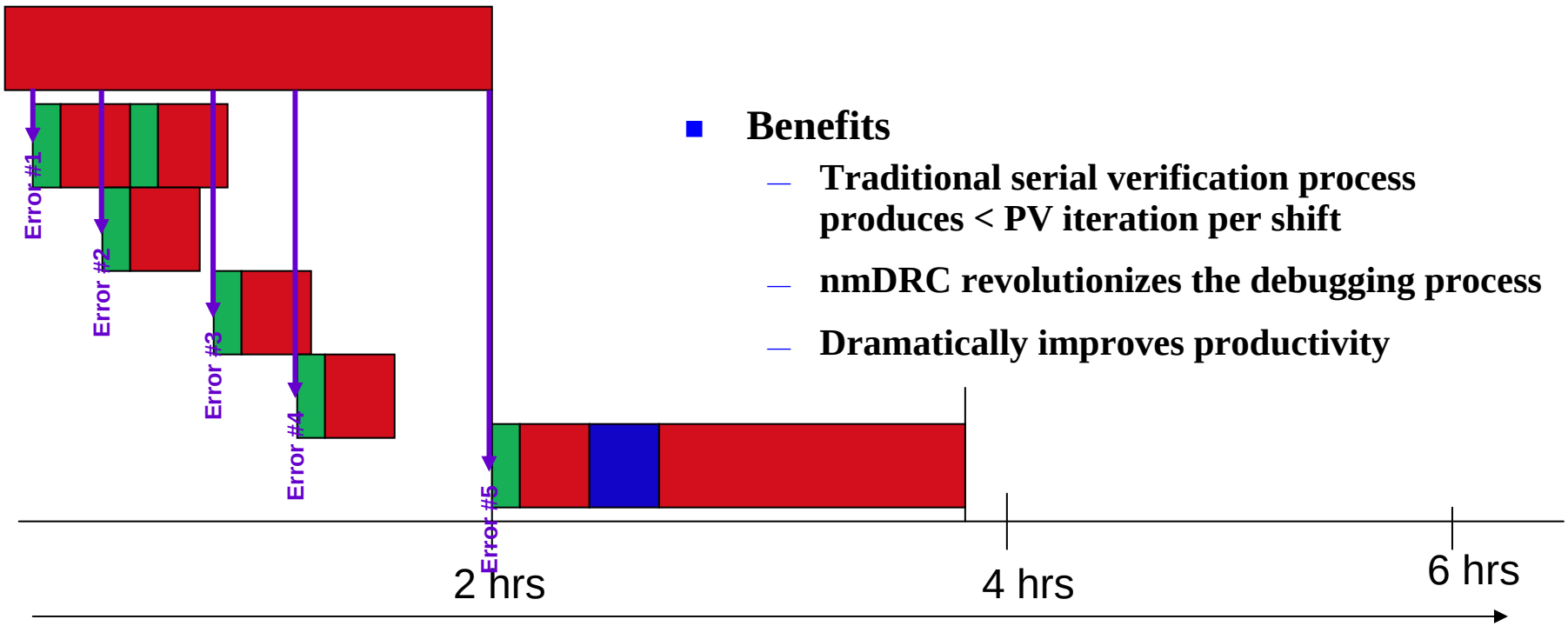


Calibre nmDRC
Dramatically Reduced Iteration Runtimes

Traditional Serial DRC Verification

Days

Calibre nmDRC: Dynamic Results Visualization and Incremental Verification



- **Benefits**
  - **Traditional serial verification process produces < PV iteration per shift**
  - **nmDRC revolutionizes the debugging process**
  - **Dramatically improves productivity**

Calibre nmDRC
Modern Development Tools

Traditional SVRF
Recommended Rule Metal1

```
METAL1.1.1R#rra#b0.28 = INT ame1 >=0.256 <0.28 ABUT >0<90 OPPOSITE REGION
METAL1.1.1R#rra#b0.30 = INT ame1 >=0.28 <0.30 ABUT >0<90 OPPOSITE REGION
METAL1.1.1R#rra#b0.32 = INT ame1 >=0.30 <0.32 ABUT >0<90 OPPOSITE REGION
METAL1.1.1R#rra#b0.28 {@ {Minimum METAL1 width >=0.256<0.28}
        DFM ANALYZE METAL1.1.1R#rra#b0.28 METAL1.1.1R#rra#b0.30 METAL1.1.1R#rra#b0.32 >=0
        [(COUNT(METAL1.1.1R#rra#b0.28))*1.0/AREA()]
        RDB ONLY "yield.rdb"
}
METAL1.1.1R#rra#b0.28_c {@ output RR yield prediction to RDB BY CELL
        @ check: METAL1.1.1R#rra
        DFM ANALYZE METAL1.1.1R#rra#b0.28 METAL1.1.1R#rra#b0.30 METAL1.1.1R#rra#b0.32 >= 0 BY CELL NOPSEUDO
        [(COUNT(METAL1.1.1R#rra#b0.28))*1.0/AREA()]
        RDB ONLY "yield.rdb"
}
METAL1.1.1R#rra#b0.28_ {@ {Minimum METAL1 width >=0.256<0.28}
        COPY METAL1.1.1R#rra#b0.28
}
METAL1.1.1R#rra#b0.30 {@ {Minimum METAL1 width >=0.28<0.30}
        DFM ANALYZE METAL1.1.1R#rra#b0.28 METAL1.1.1R#rra#b0.30 METAL1.1.1R#rra#b0.32 >=0
        [(COUNT(METAL1.1.1R#rra#b0.30))*0.8/AREA()]
        RDB ONLY "yield.rdb"
}
METAL1.1.1R#rra#b0.30_c {@ output RR yield prediction to RDB BY CELL
        @ check: METAL1.1.1R#rra
        DFM ANALYZE METAL1.1.1R#rra#b0.28 METAL1.1.1R#rra#b0.30 METAL1.1.1R#rra#b0.32 >= 0 BY CELL NOPSEUDO
        [(COUNT(METAL1.1.1R#rra#b0.30))*0.8/AREA()]
        RDB ONLY "yield.rdb"
}
METAL1.1.1R#rra#b0.30_ {@ {Minimum METAL1 width >=0.28<0.30}
        COPY METAL1.1.1R#rra#b0.30
}
METAL1.1.1R#rra#b0.32 {@ {Minimum METAL1 width >=0.30<0.32}
        DFM ANALYZE METAL1.1.1R#rra#b0.28 METAL1.1.1R#rra#b0.30 METAL1.1.1R#rra#b0.32 >=0
        [(COUNT(METAL1.1.1R#rra#b0.32))*0.6/AREA()]
        RDB ONLY "yield.rdb"
}
METAL1.1.1R#rra#b0.32_c {@ output RR yield prediction to RDB BY CELL
        @ check: METAL1.1.1R#rra
        DFM ANALYZE METAL1.1.1R#rra#b0.28 METAL1.1.1R#rra#b0.30 METAL1.1.1R#rra#b0.32 >= 0 BY CELL NOPSEUDO
        [(COUNT(METAL1.1.1R#rra#b0.32))*0.6/AREA()]
        RDB ONLY "yield.rdb"
}
METAL1.1.1R#rra#b0.32_ {@ {Minimum METAL1 width >=0.30<0.32}
        COPY METAL1.1.1R#rra#b0.32
}
METAL1.1.1R#rra# {@ {Minimum METAL1 width}
        DFM ANALYZE METAL1.1.1R#rra#b0.28 METAL1.1.1R#rra#b0.30 METAL1.1.1R#rra#b0.32 >=0
        [((COUNT(METAL1.1.1R#rra#b0.28))*1.0+(COUNT(METAL1.1.1R#rra#b0.30))*0.8+(COUNT(METAL1.1.1R#rra#b0.32))*0.6)/AREA()]
        RDB ONLY "yield.rdb"
}
METAL1.1.1R#rra#_c {@ output RR yield prediction to RDB BY CELL
        @ check: METAL1.1.1R#rra
        DFM ANALYZE METAL1.1.1R#rra#b0.28 METAL1.1.1R#rra#b0.30 METAL1.1.1R#rra#b0.32 >= 0 BY CELL NOPSEUDO
        [((COUNT(METAL1.1.1R#rra#b0.28))*1.0+(COUNT(METAL1.1.1R#rra#b0.30))*0.8+(COUNT(METAL1.1.1R#rra#b0.32))*0.6)/AREA()]
        RDB ONLY "yield.rdb"
}
```

Repeat For Metal2 through Metal9

Total Lines of SVRF Code = 509

Calibre TVF
Recommended Rule Metal1

```
set met111_bin {SLIST 0.256 0.28 0.30 0.32}
Create_RRA_SVRF METAL1.1.1R {WID_MIN_L1 {ame1 ORTHO} "Minimum METAL1 width"} \
        $met111_bin {DLIST 1.0 0.8 0.6} {USER $lambda/AREA()}
```

Call Template = 2 lines of TVF Code

Library Template = 59 lines of TVF Code

Forloop all metals = 3 lines of TVF Code

Total lines of TVF Code = 64

- **High level programming language**
- **Simplifies the development and maintenance of advanced rule files**

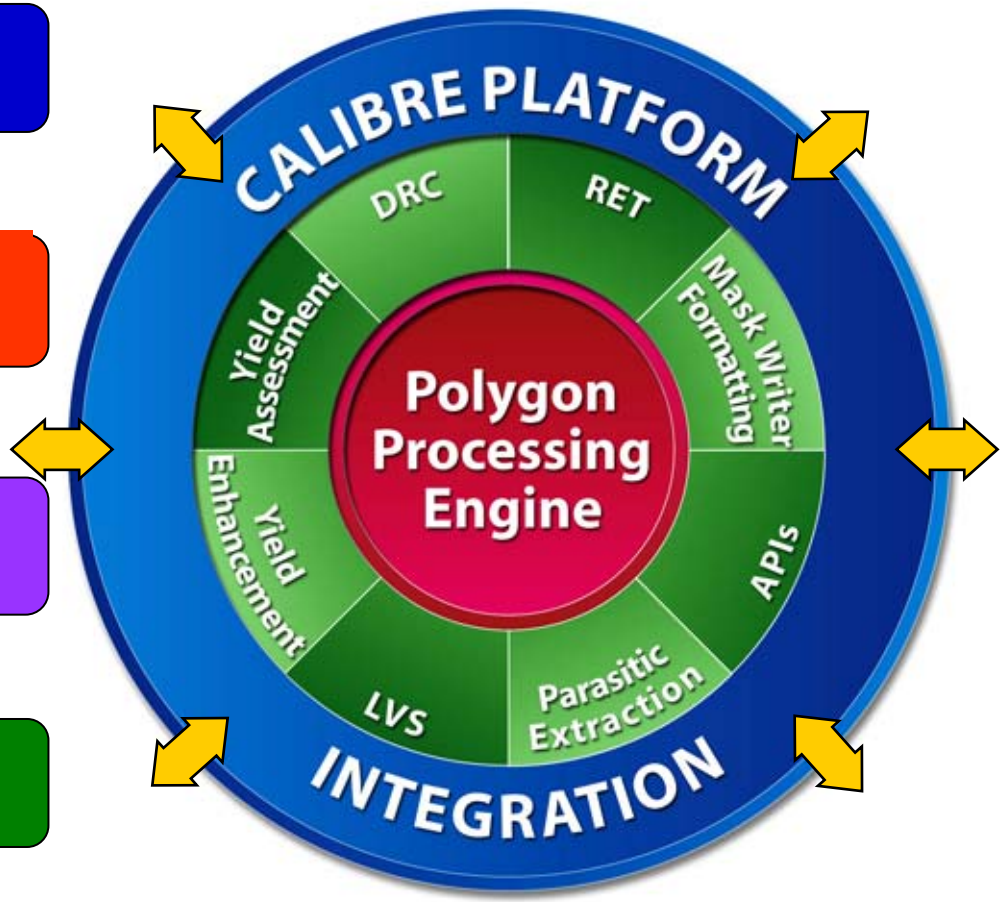
Calibre Integrated into Design Platforms

Mentor
IC Station, DESIGNrev

Cadence
Virtuoso/ADE, Encounter

Synopsys
Astro

Magma
BlastFusion



GDSII

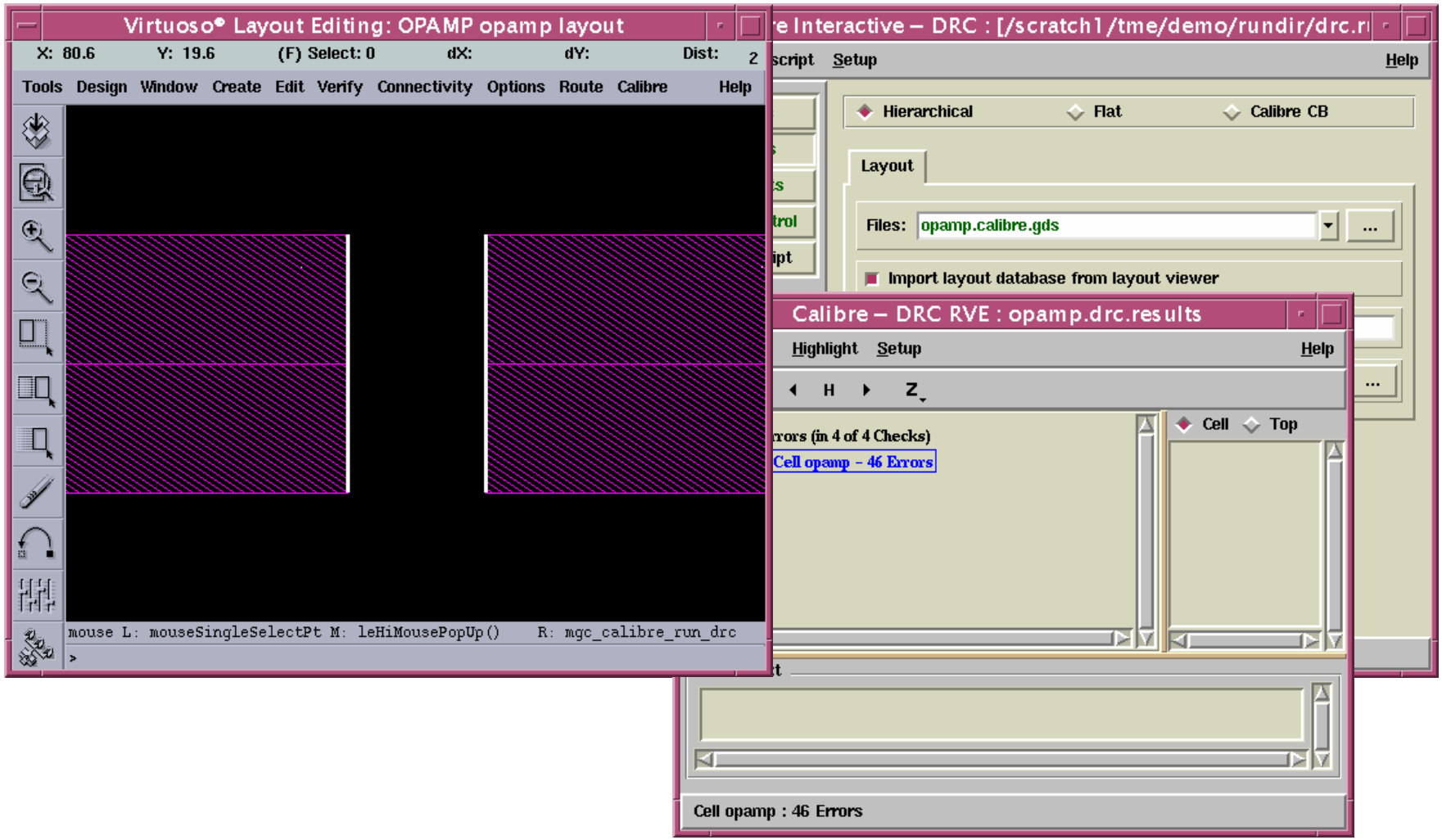
OASIS

Milkyway

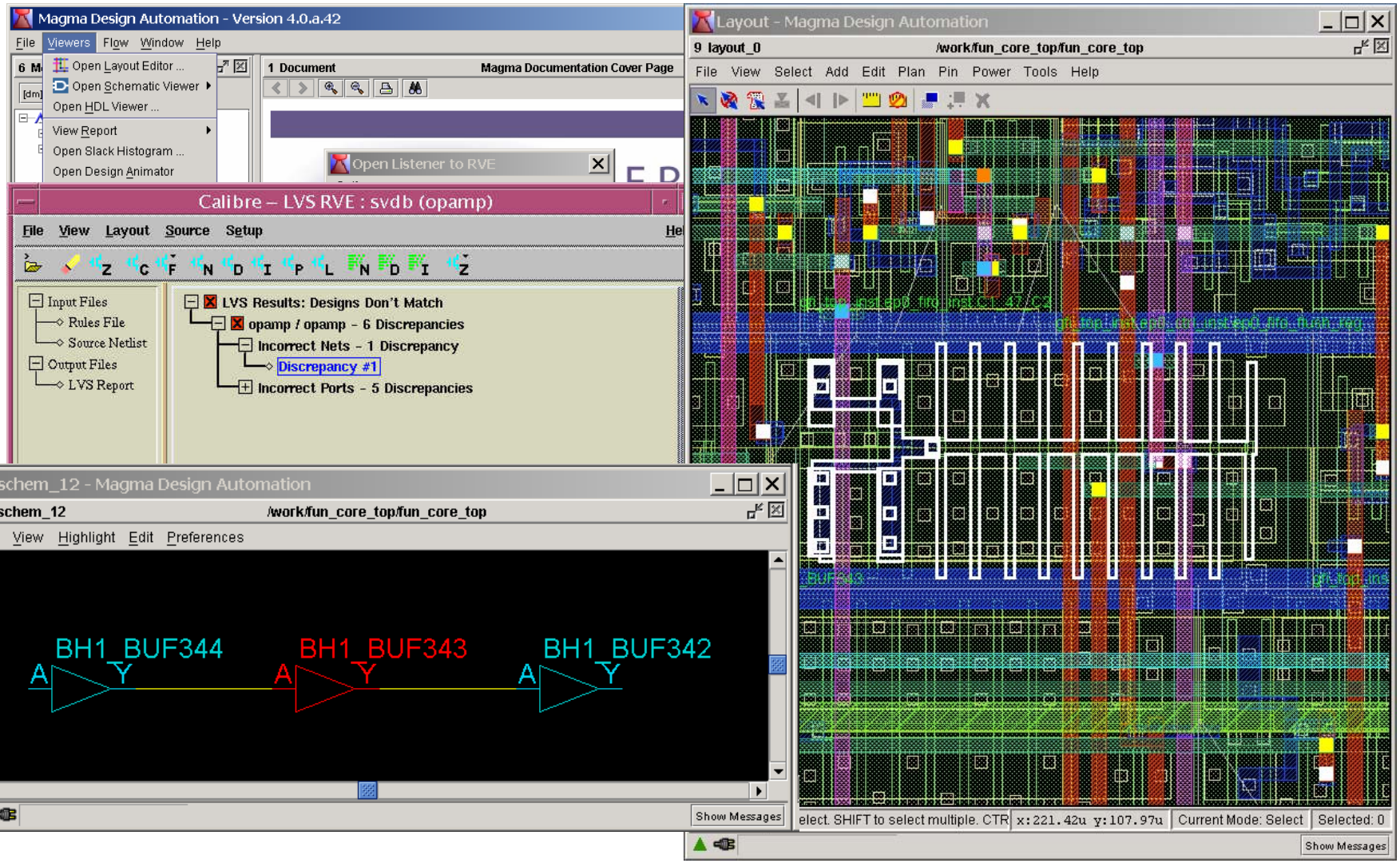
OpenAccess

LEF/DEF

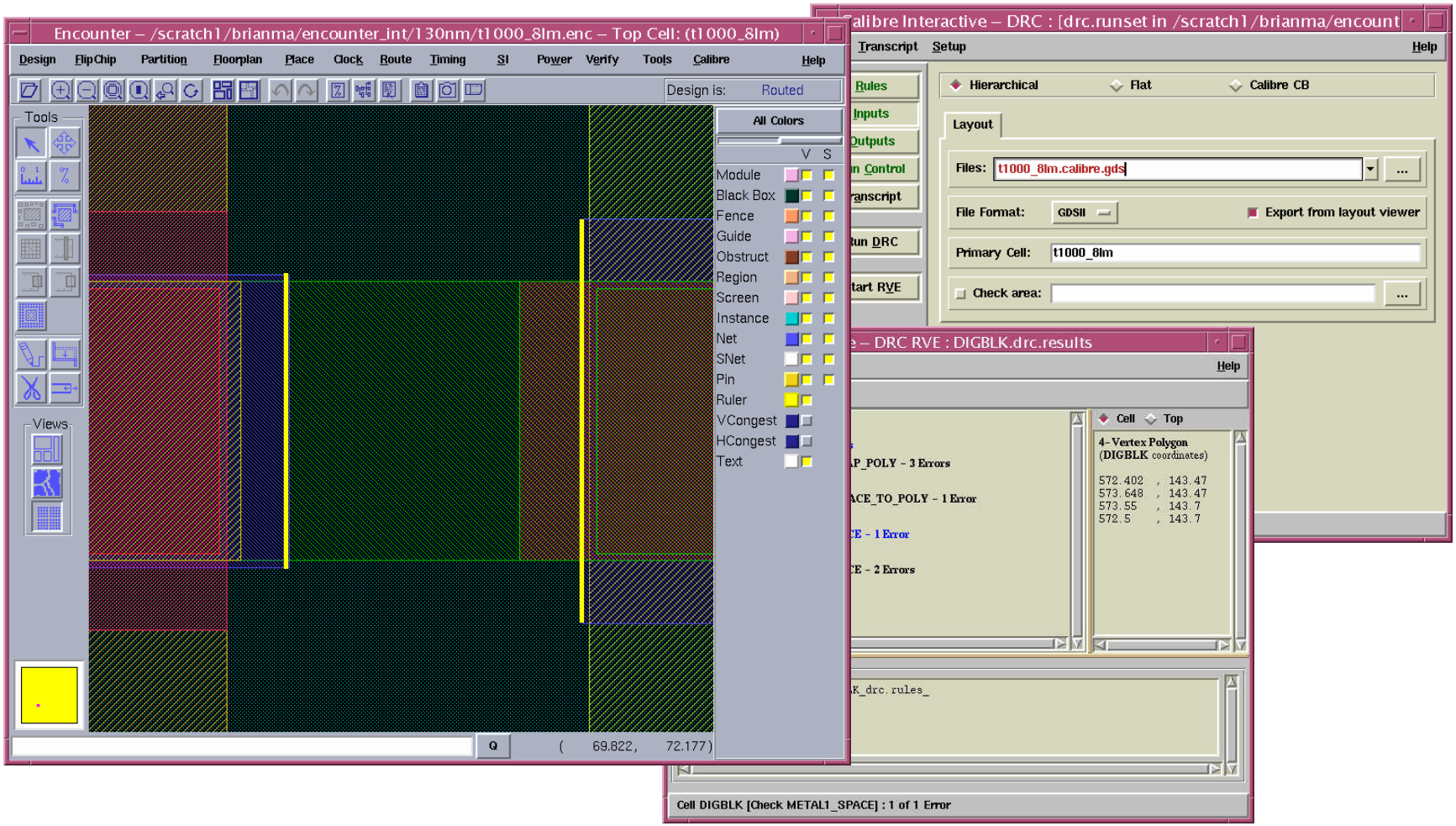
Virtuoso Integration Example



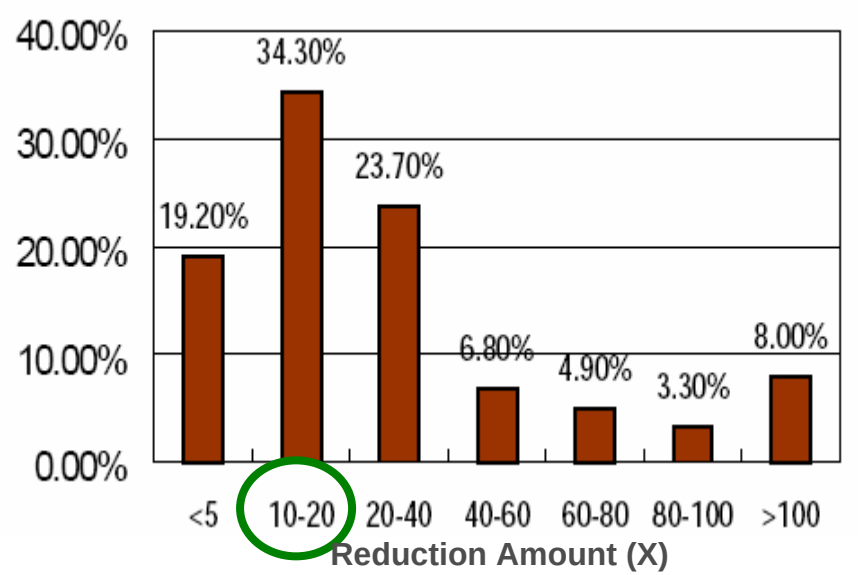
BlastFusion Integration Example



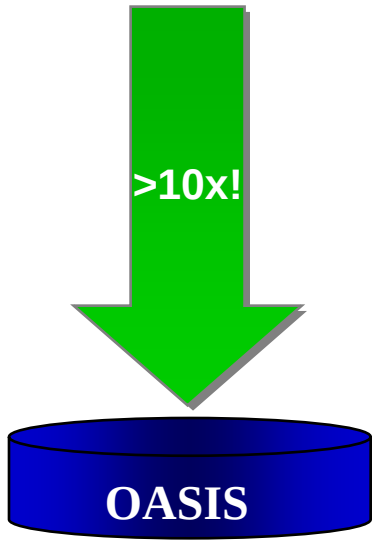
Encounter Integration Example



OASIS: Tackling the Capacity Bottlenecks

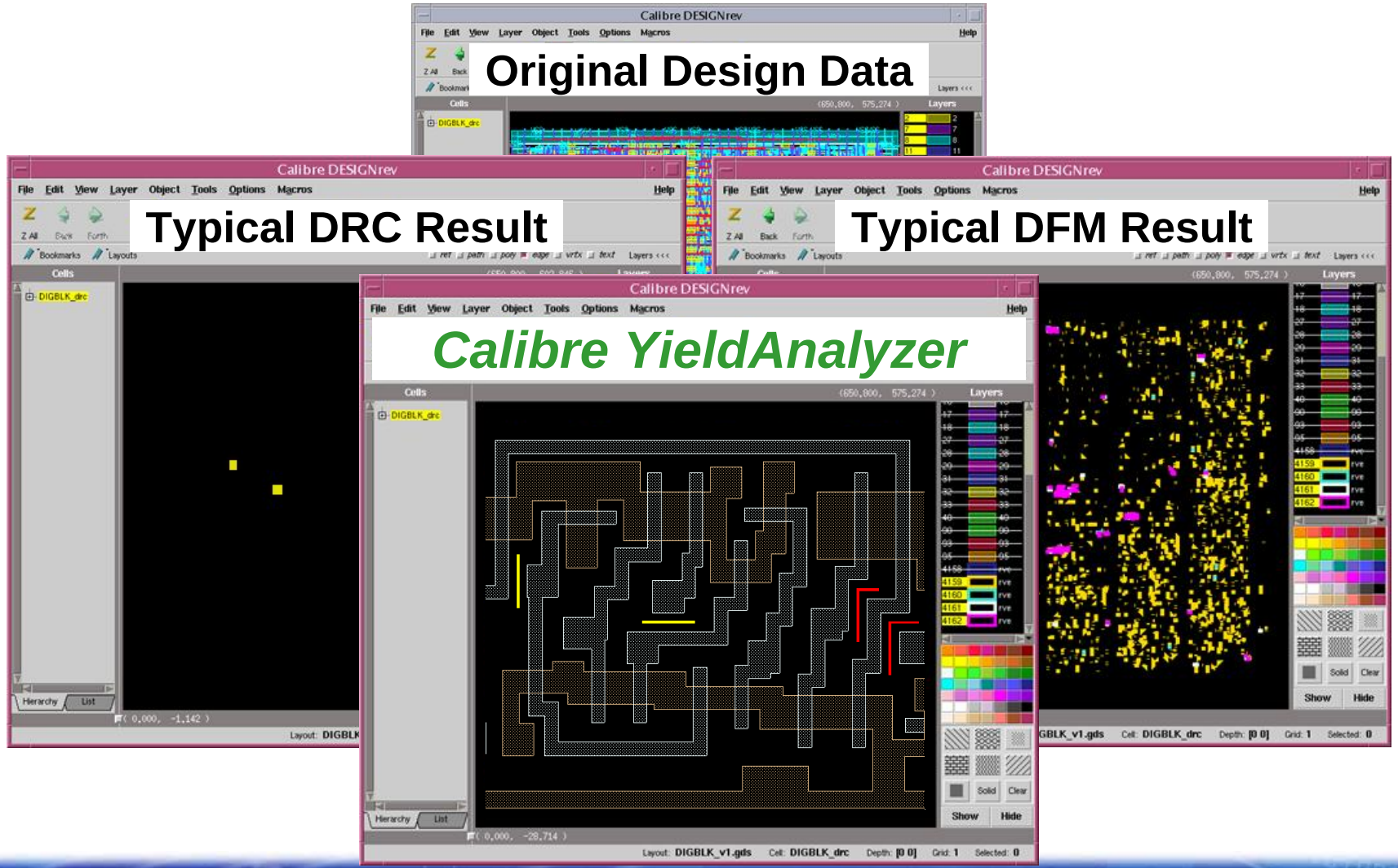


Original GDSII-to-OASIS
File Size Reduction Distribution

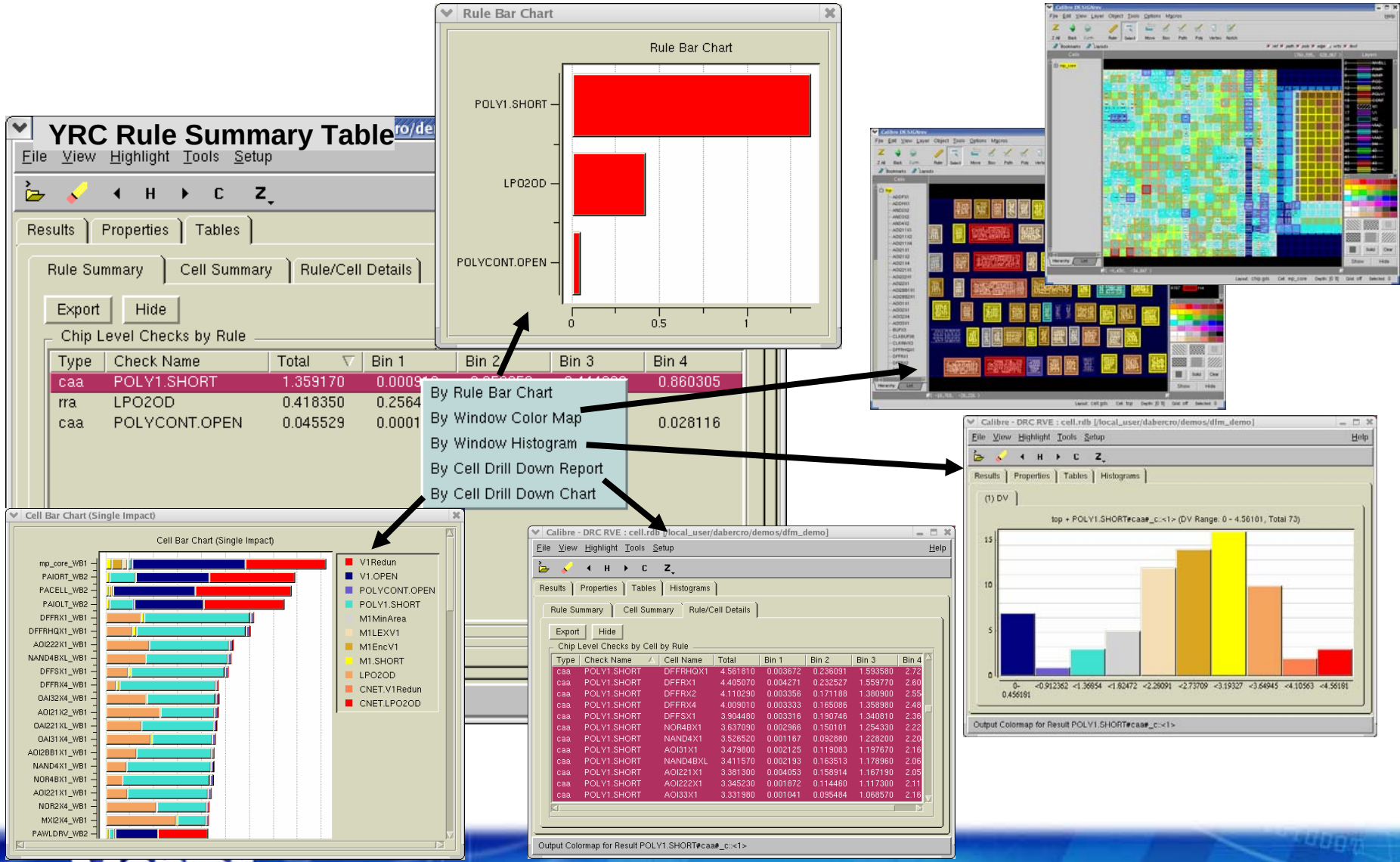


Evaluation of 5000 customer GDSII vs OASIS data files!

Statistical Analysis Augments Simple Error Markers

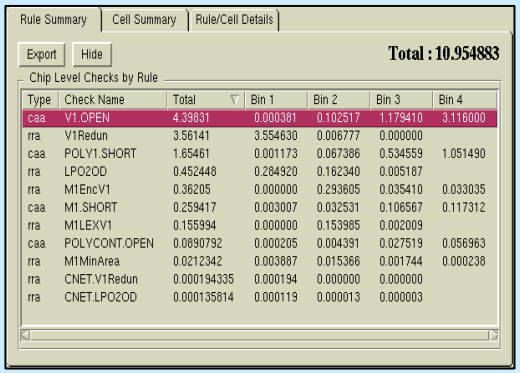


Yield Analysis and Visualization

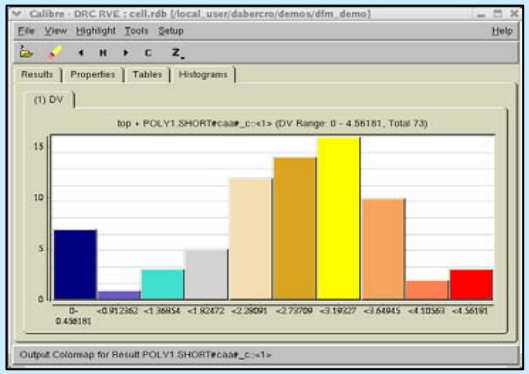


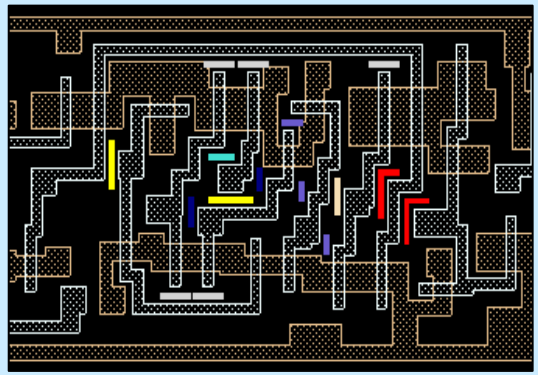
Model Based Verification: From DRC to nmDRC

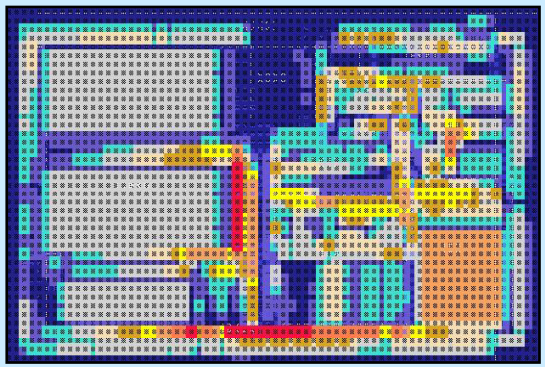
	Random	*Systematic*	*Parametric*
Rule Based	**Calibre YieldAnalyzer** **Recommended Rule Analysis**	**Calibre YieldAnalyzer** **Recommended Rule Analysis**	**Calibre YieldAnalyzer** **Recommended Rule Analysis**
Model Based	**Calibre YieldAnalyzer** **Critical Area Analysis**	**Calibre LFD** **Litho Variation Analysis**	**Calibre LVS/xRC/xL** **Mfg Aware Silicon Modeling**

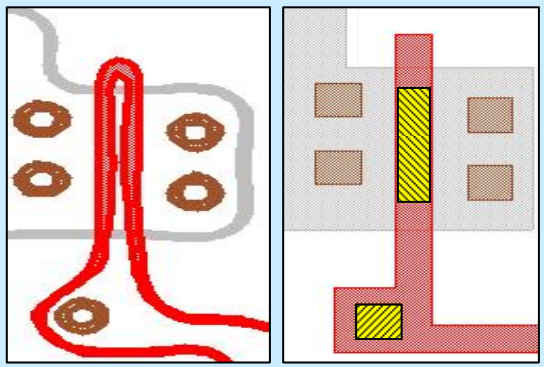


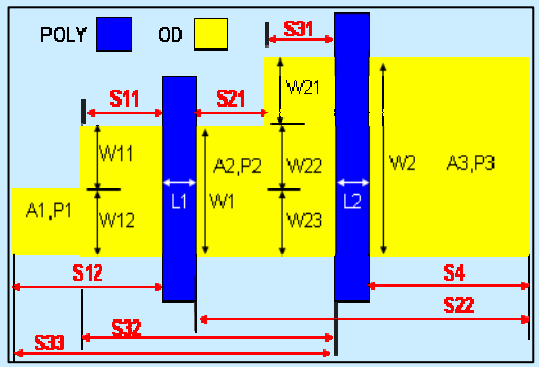
Type	Check Name	Total	Bin 1	Bin 2	Bin 3	Bin 4
caa	V1.OPEN	4.39831	0.000381	0.102517	1.173410	3.116000
rra	V1Redun	3.56141	3.554630	0.006777	0.000000	
caa	POLY1.SHORT	1.65461	0.001173	0.067386	0.534559	1.051490
rra	LPO2OD	0.452448	0.284920	0.162340	0.005187	
rra	M1EncV1	0.36205	0.000000	0.293605	0.035410	0.033035
caa	M1.SHORT	0.259417	0.003007	0.032531	0.106567	0.117312
rra	M1LEXV1	0.155994	0.000000	0.153985	0.002009	
caa	POLYCONT.OPEN	0.0890792	0.000205	0.004391	0.027519	0.056963
rra	M1MinArea	0.0212342	0.003887	0.015366	0.001744	0.000238
rra	CNET.V1Redun	0.000194335	0.000194	0.000000	0.000000	
rra	CNET.LPO2OD	0.000135814	0.000119	0.000013	0.000003	







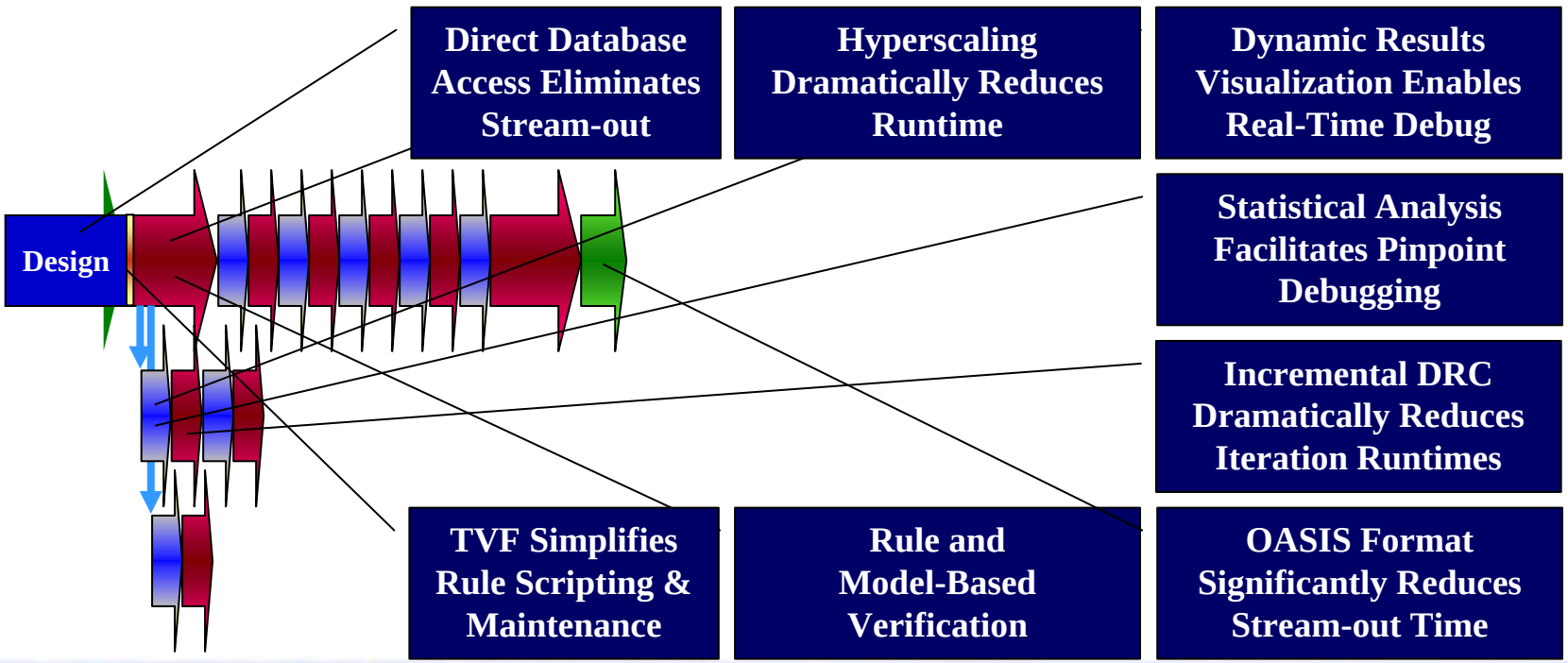




Solving the WHOLE Cycle Time Issue

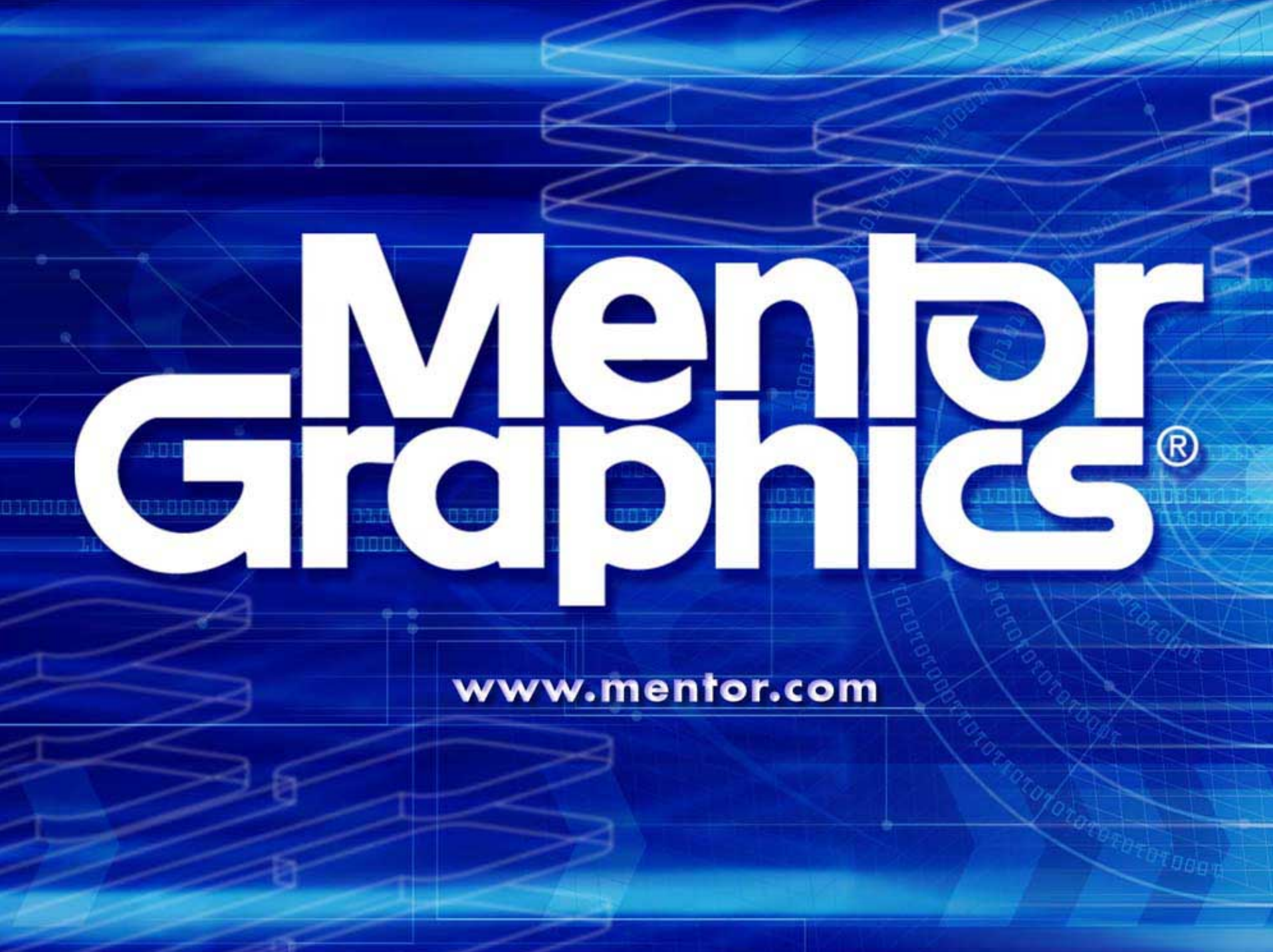
Classic Serial Verification

nmDRC Verification



Summary

- **The Calibre nm Platform provides the industry's most robust platform for design to silicon in the DFM era**
- **With Calibre nmDRC we continue to provide best in class performance, improved total TAT and the design database integration required for nanometer design**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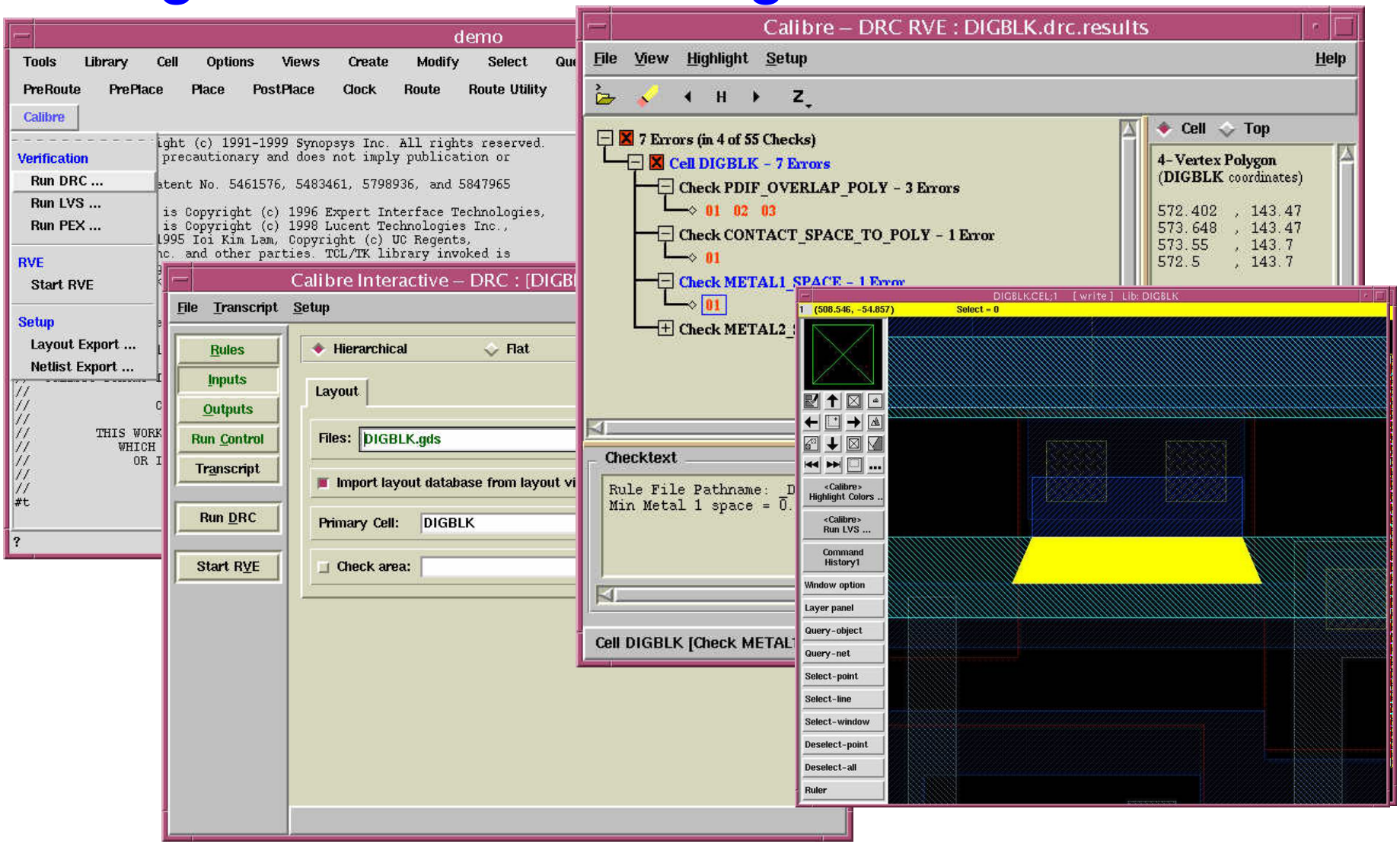
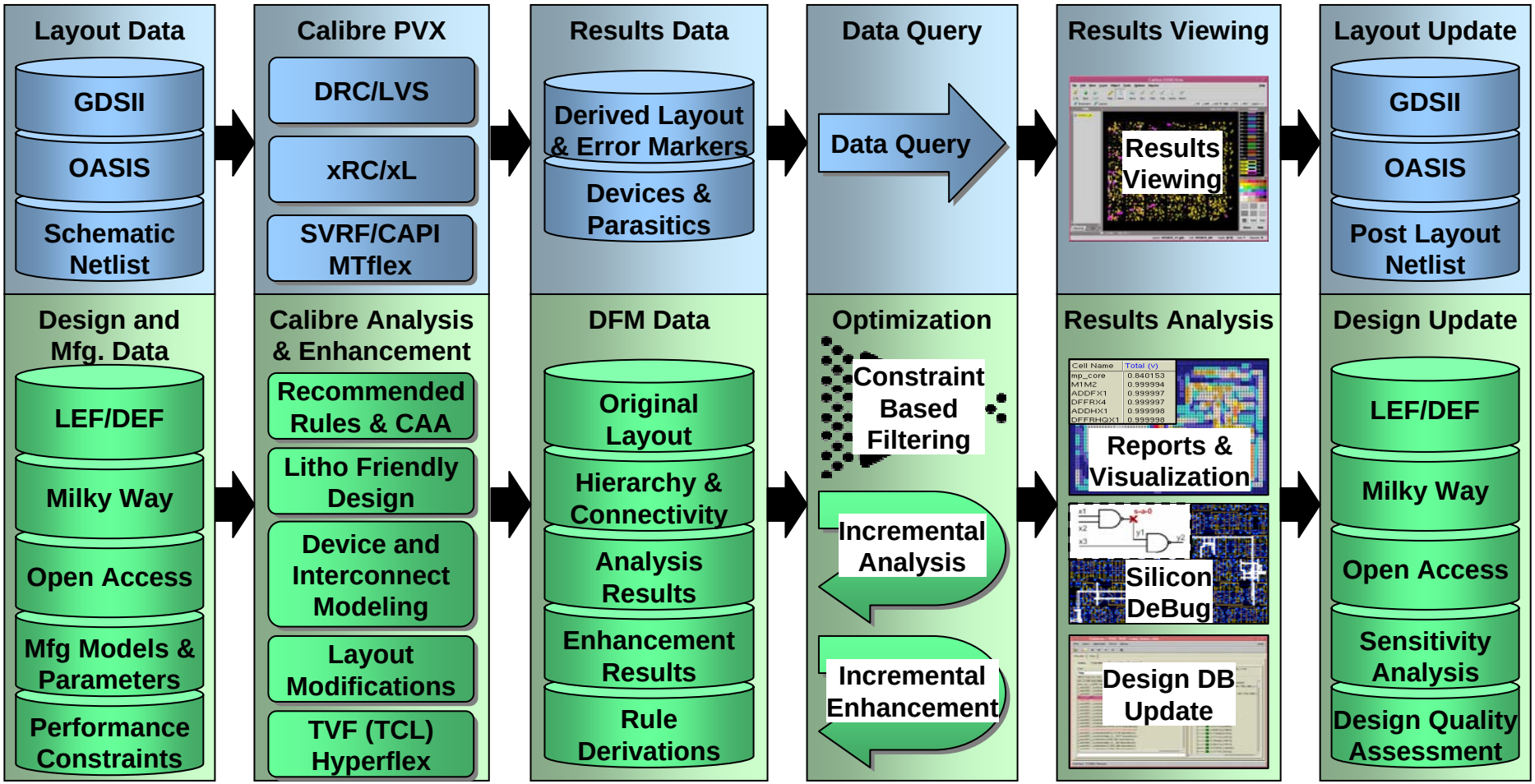
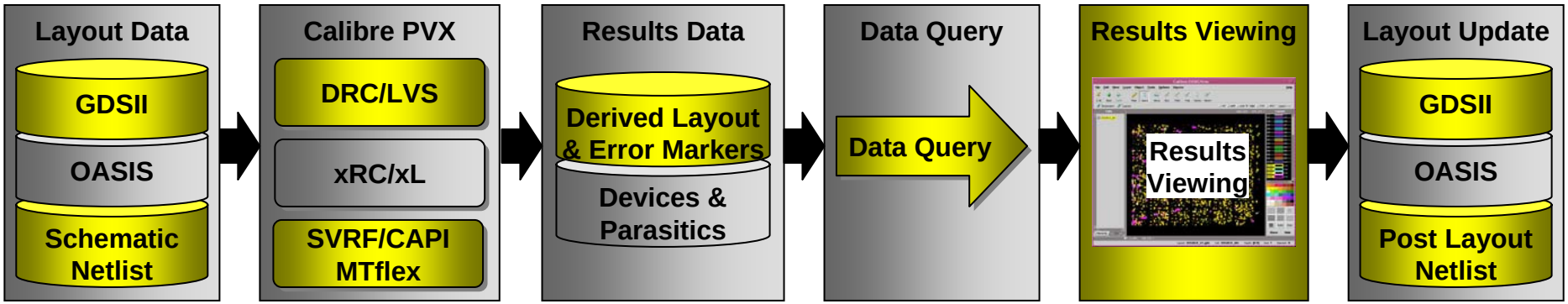
Design Environment Integration: How It Works



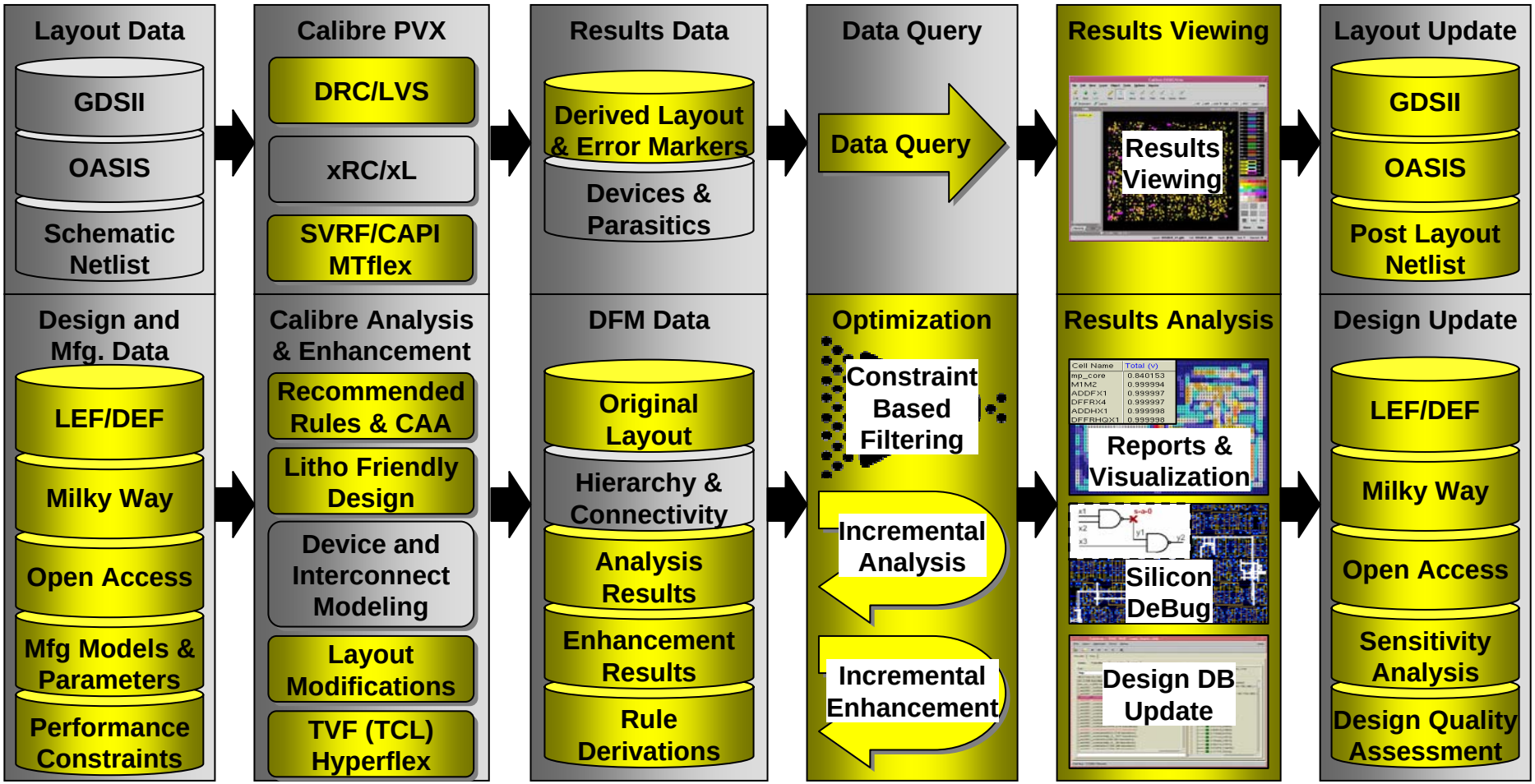
Introducing the New Calibre nm Platform



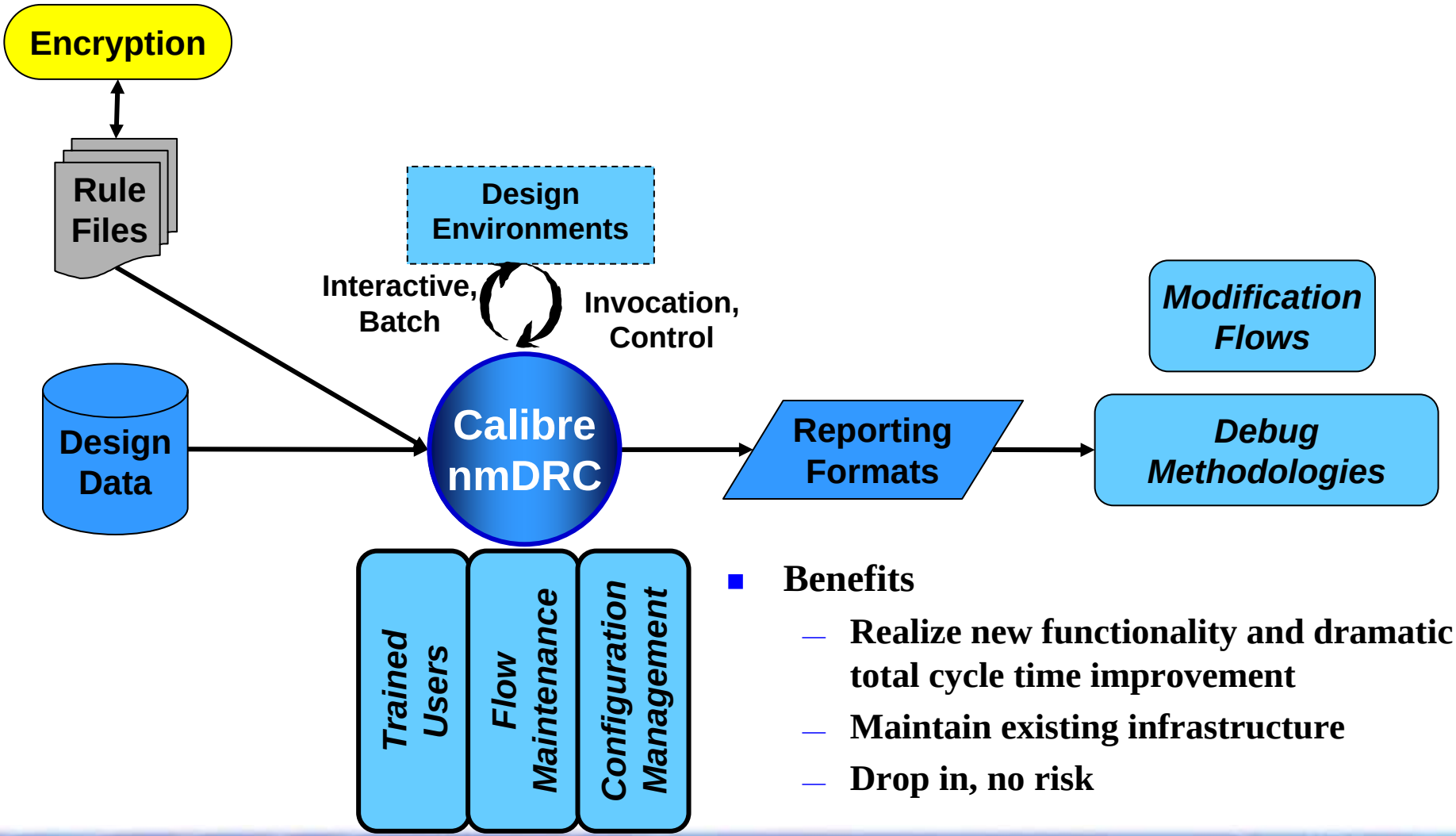
Traditional DRC



Introducing Next Generation DRC Calibre nmDRC

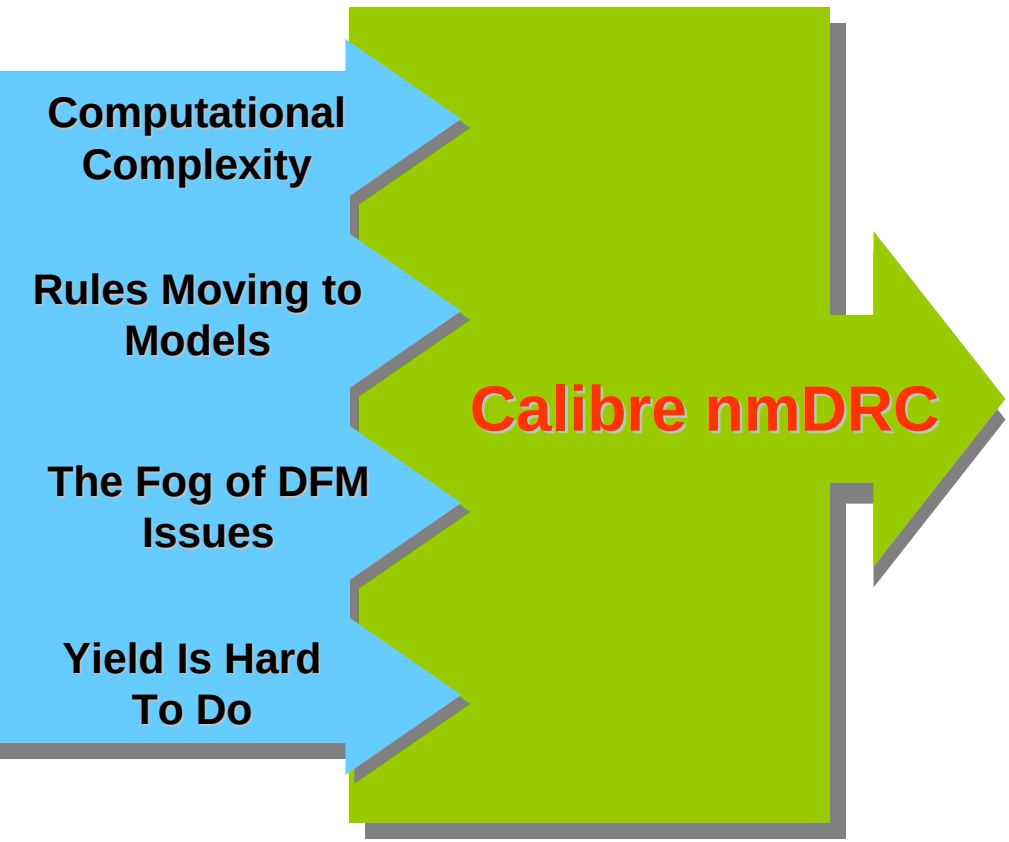


Calibre nmDRC: Drops Into Current CAD Environment Without Disruption



- **Benefits**
  - Realize new functionality and dramatic total cycle time improvement
  - Maintain existing infrastructure
  - Drop in, no risk

Advantages of Calibre nmDRC



- **Faster Turn Around Time**
- **Modern Development Tools**
- **Model-Based Verification**
- **Statistical Analysis to Augment Simple Error Markers**
- **Integration that allows tight 'fix' loops**
- **Higher productivity**