

Introducing: The Calibre nm Platform and Calibre nmDRC

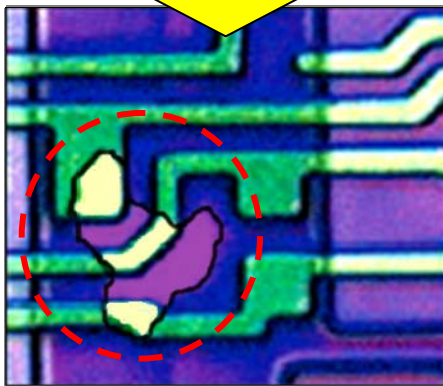
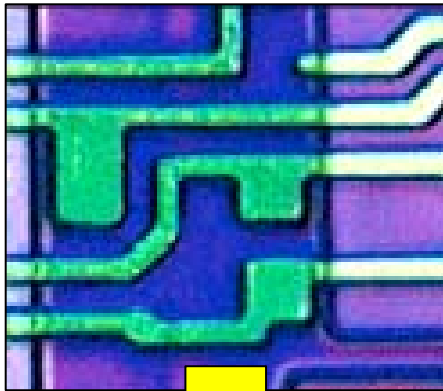
Joe Sawicki

VP and GM, Design to Silicon Division

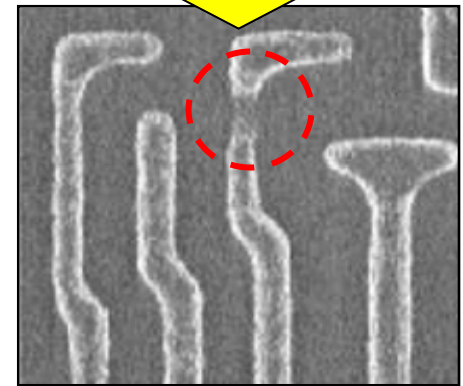
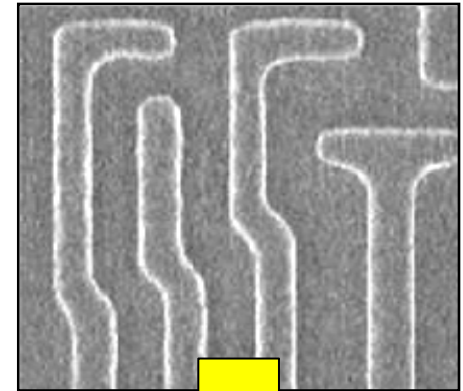
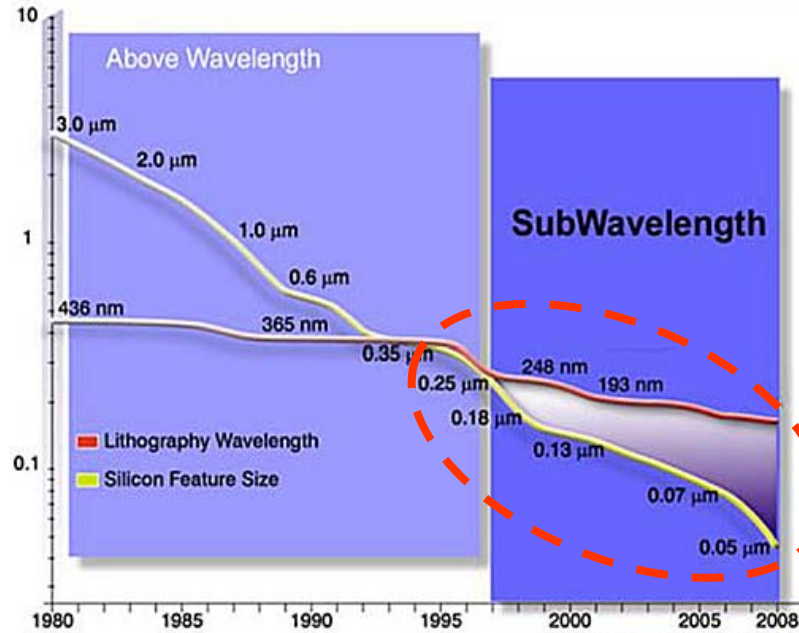
June/July 2006

**Mentor
Graphics®**

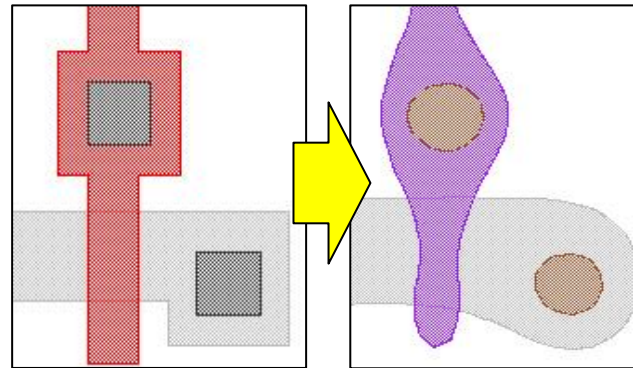
Yield Issues in Nanometer Technologies



Random



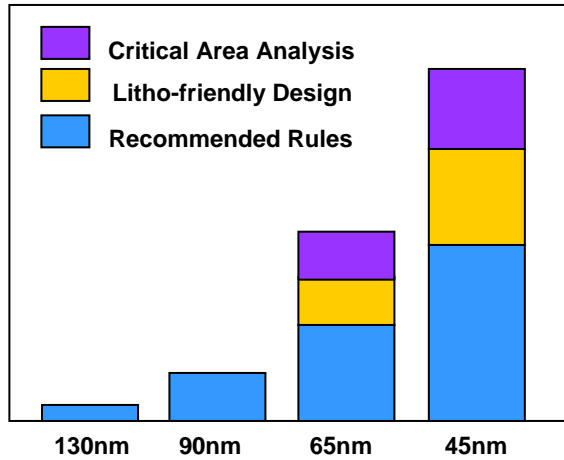
Systematic



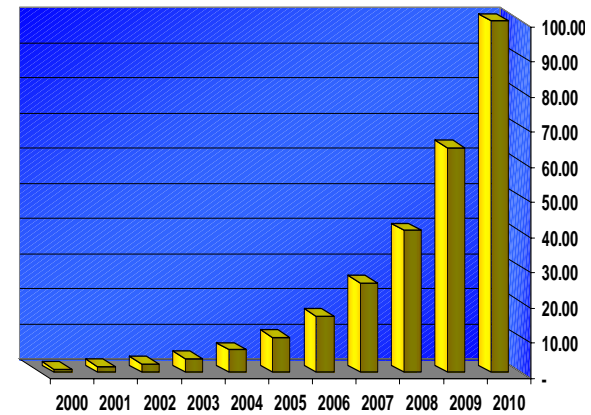
Parametric

The Wonderful and Frightening World of Physical Verification and DFM

Additional DFM Rules

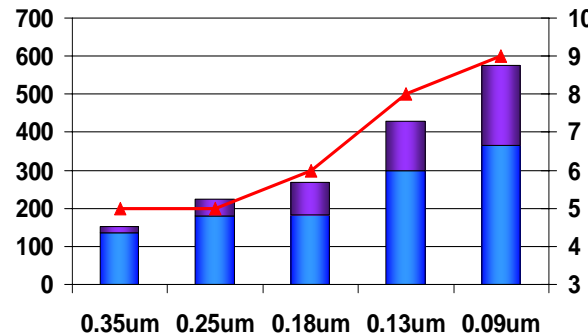


Total Geometric Shape Count



Design Size (Geometry Count)

■ Rules with 3 metal layers ■ Additional metal rules
▲ Total DRC rules



Basic DRC Rules

Computational Complexity

Additional DFM Rules



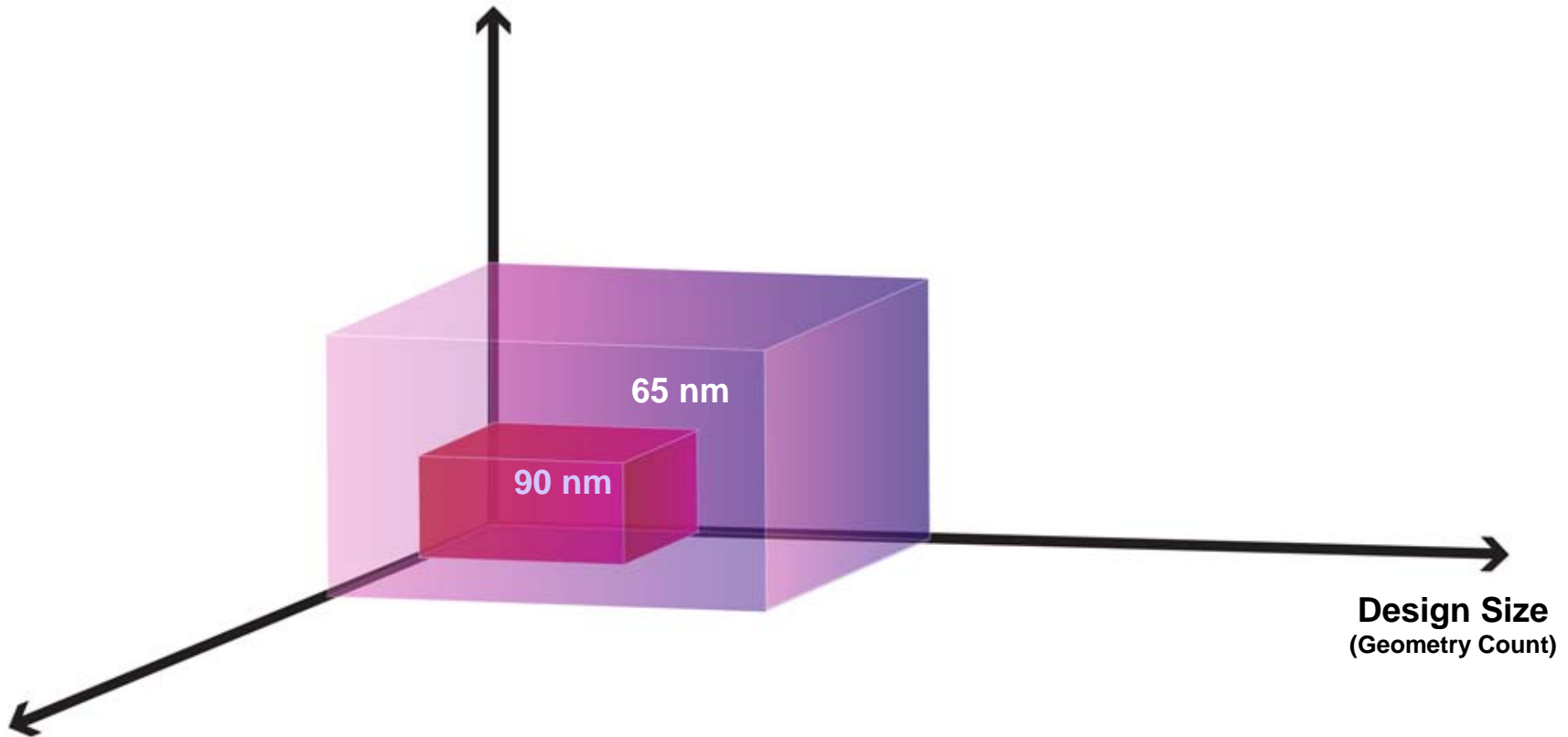
90 nm

Design Size
(Geometry Count)

Basic DRC Rules

Computational Complexity

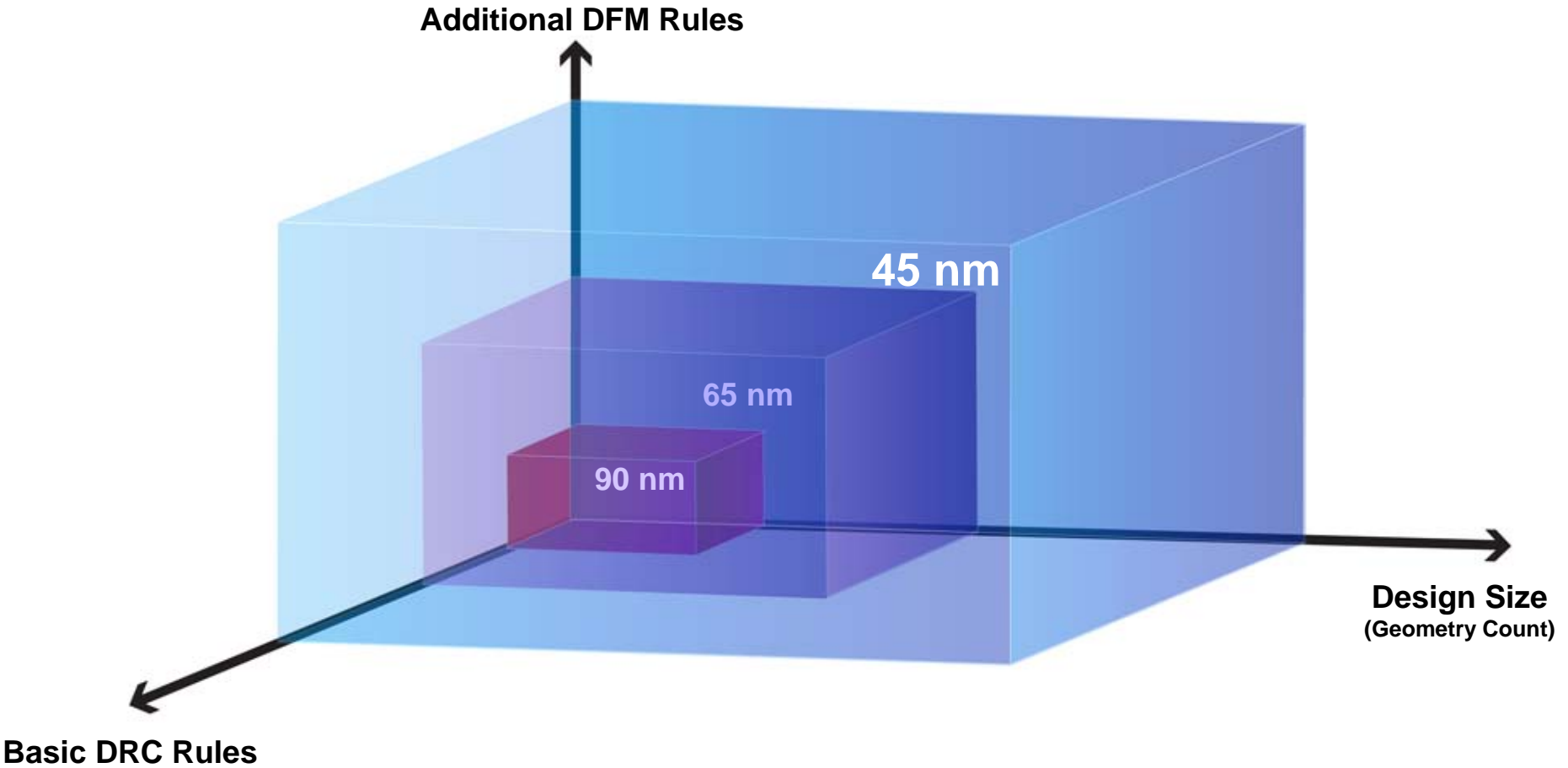
Additional DFM Rules



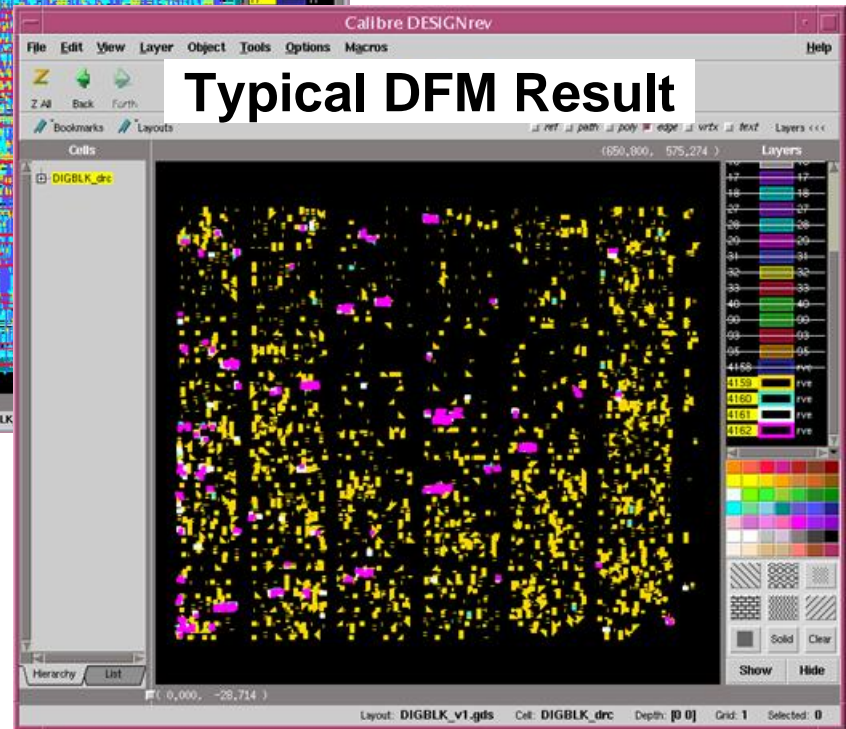
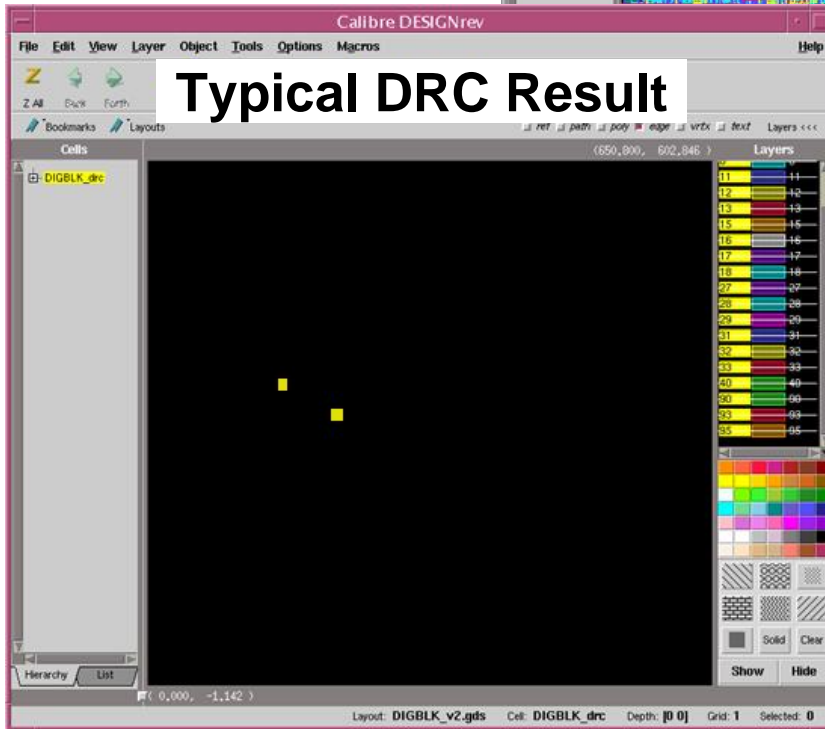
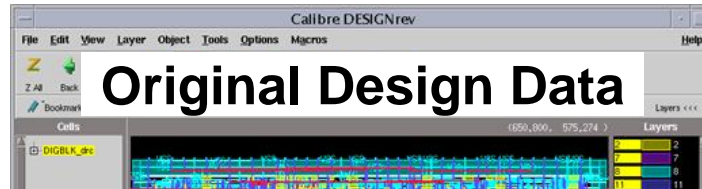
Design Size
(Geometry Count)

Basic DRC Rules

Computational Complexity

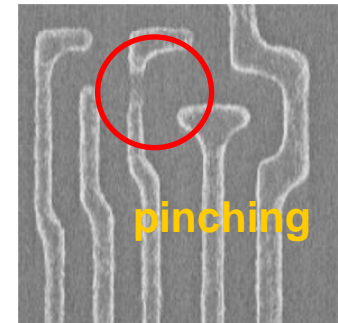
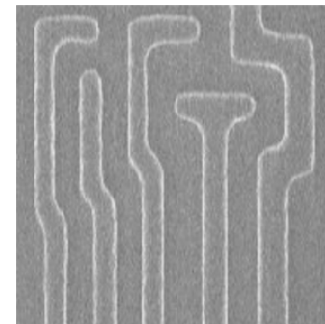
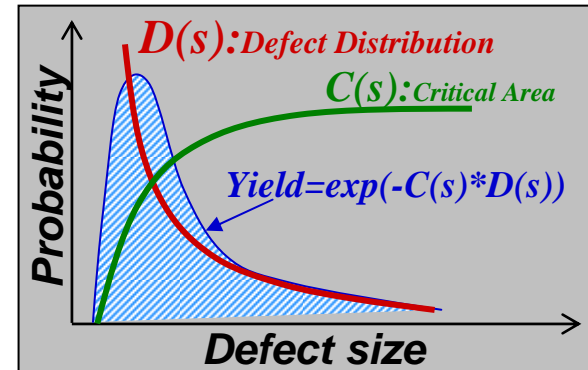


Design: Seeing through the Fog



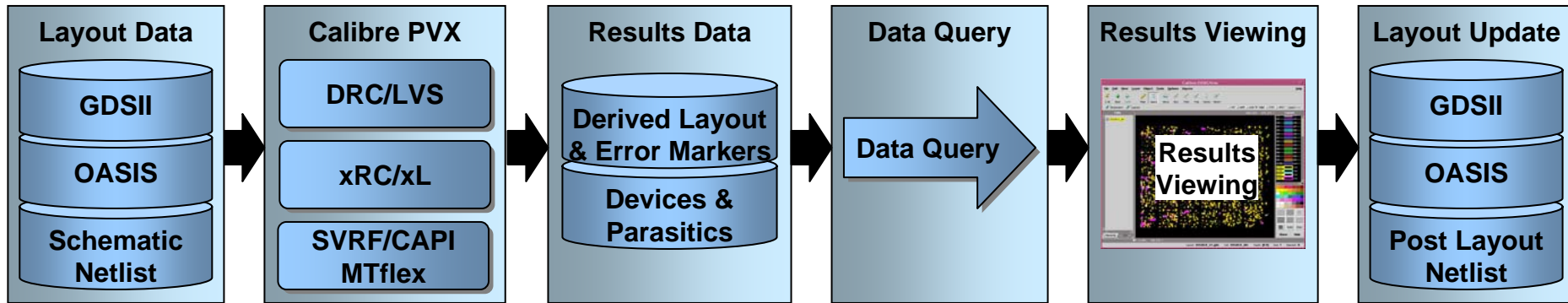
Complexity Drives a Change From Rules to Models

- Major DFM capabilities are moving from a rules-based approach to a models-based approach
 - Critical Area Analysis (CAA)
 - Litho-friendly Design (LFD)

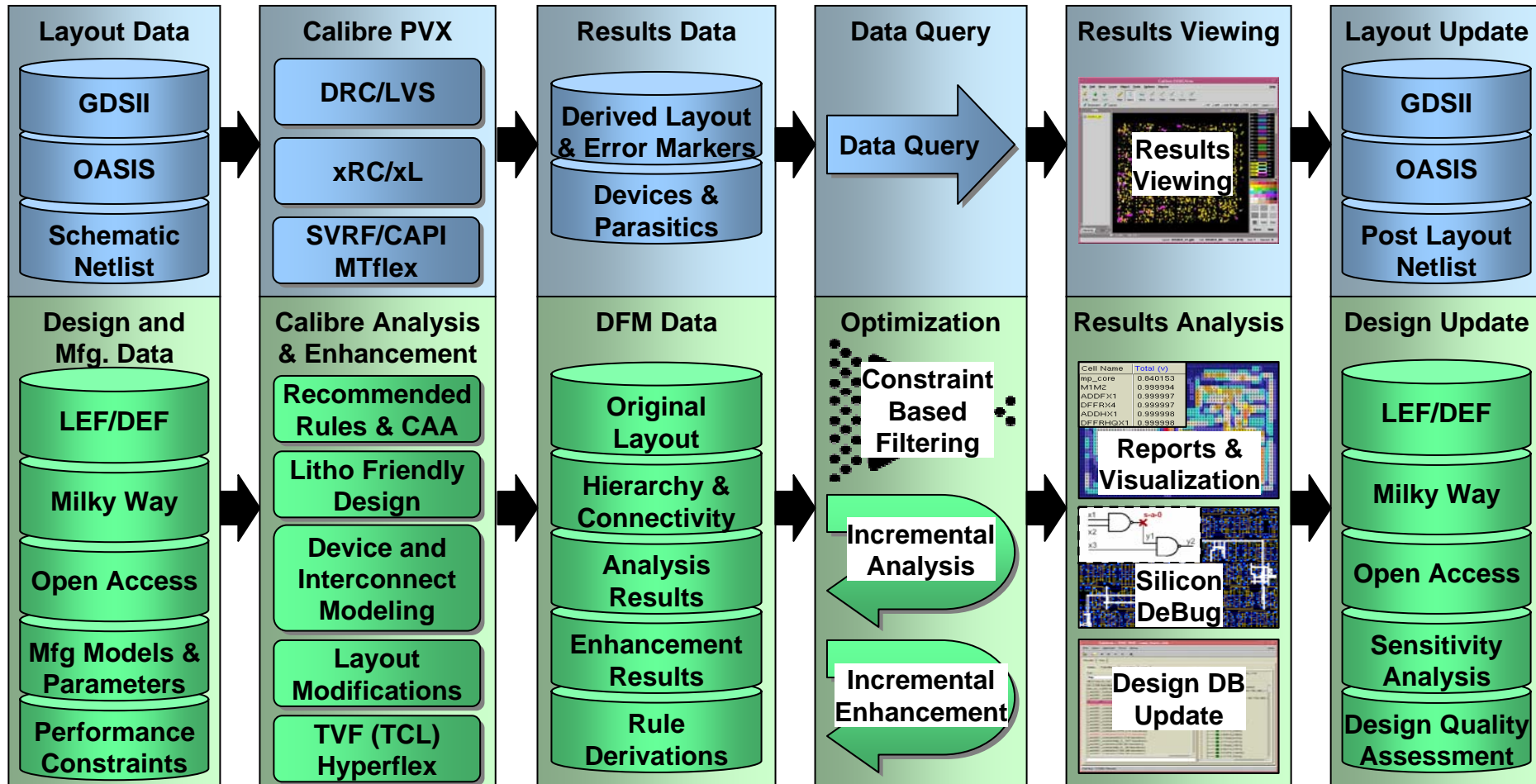


Increasing complexity and the rise in multiple issues will force this trend to continue.

Yesterday's Calibre Platform

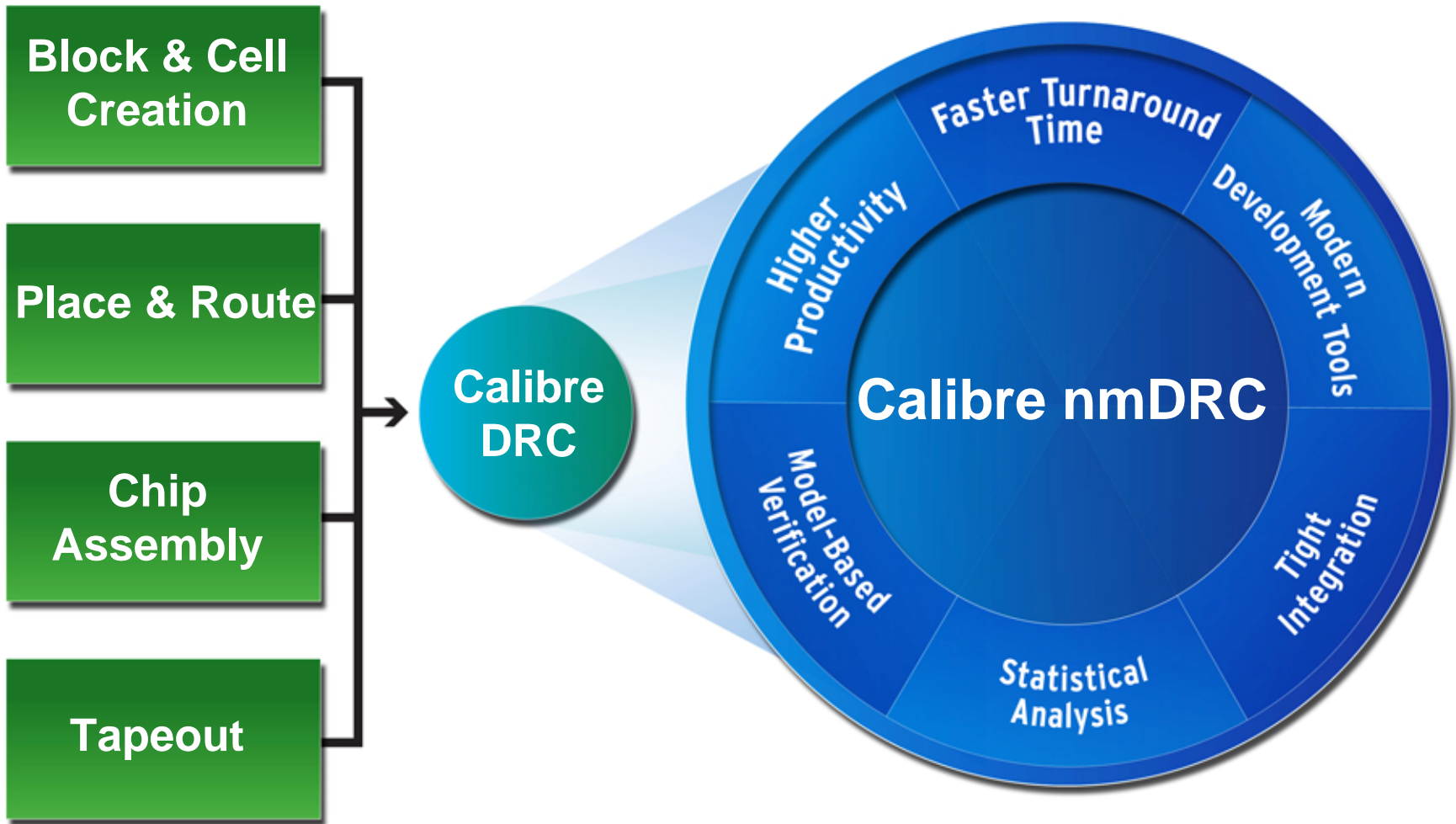


The New Calibre nm Platform

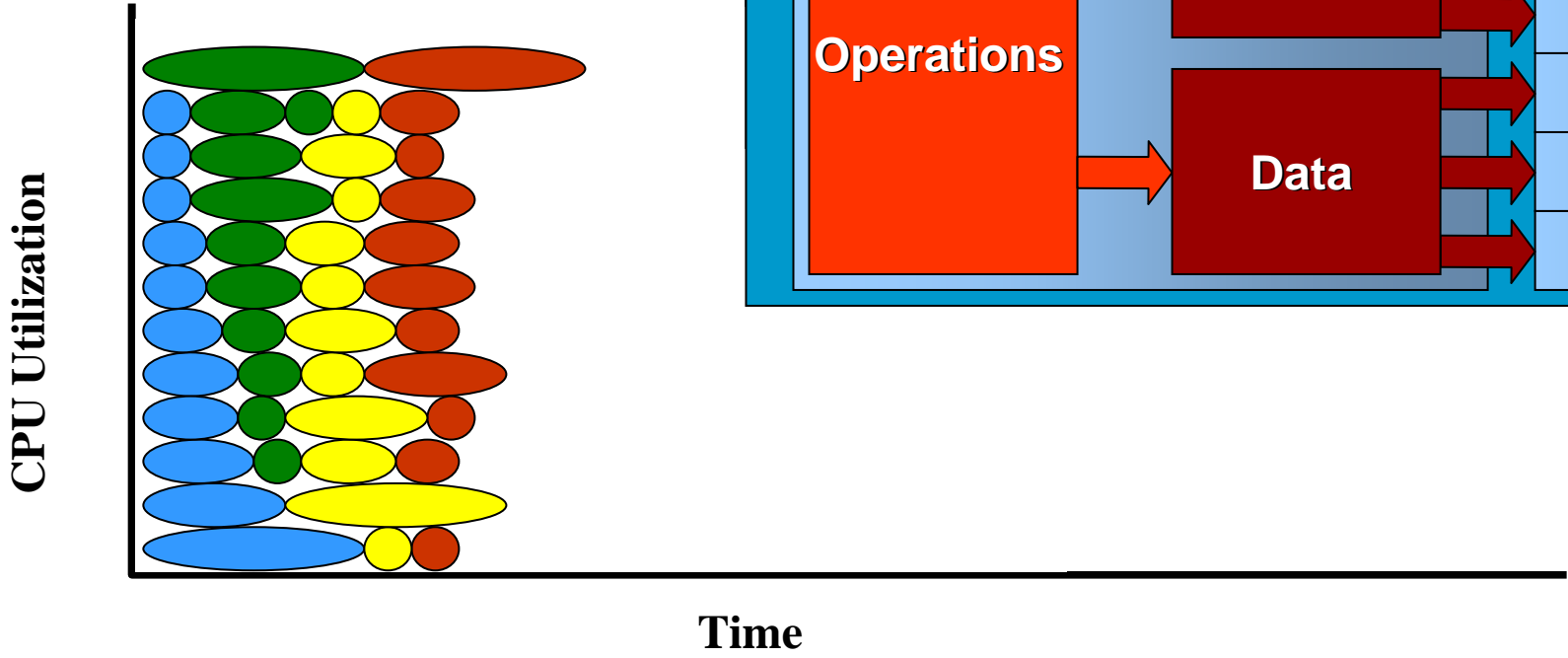
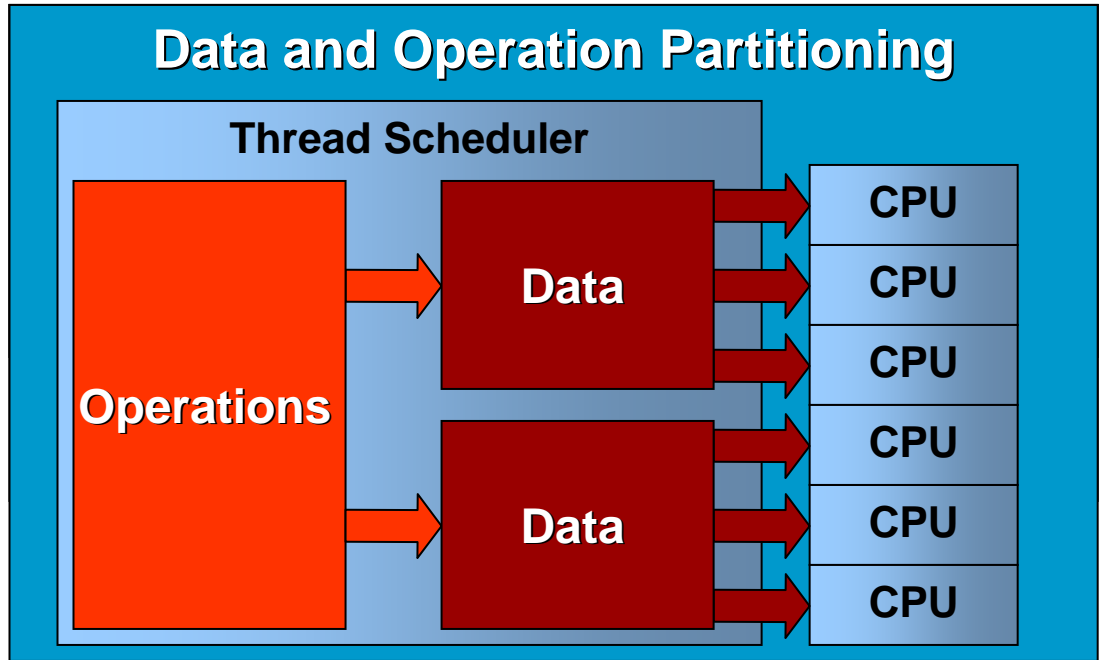


Calibre nm Platform

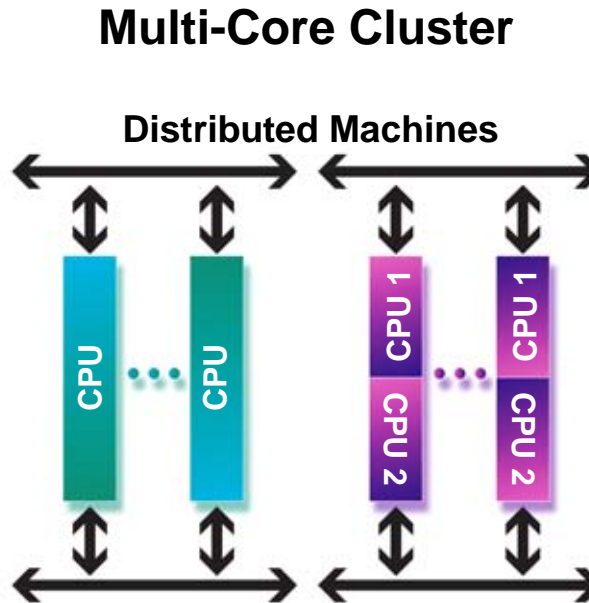
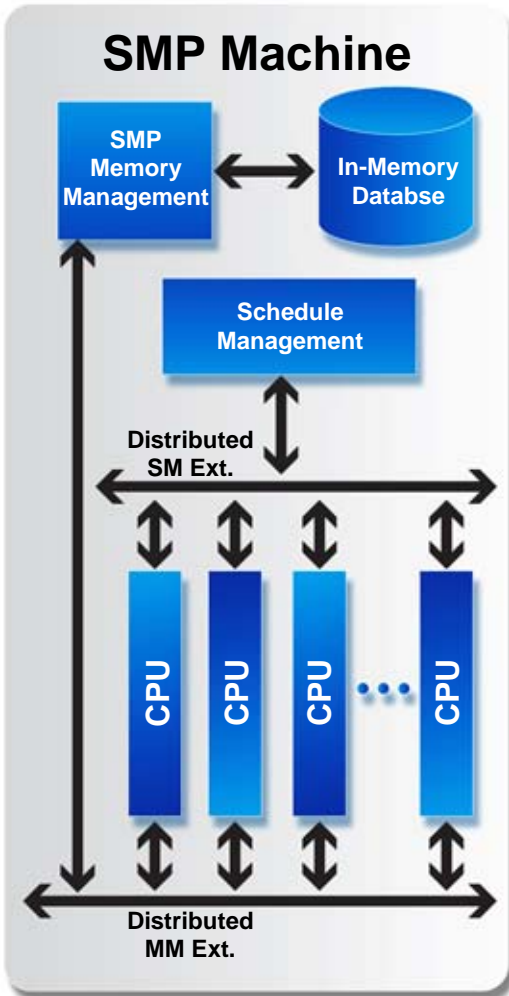
Introducing Calibre nmDRC



Achieving Faster Turn Around Times (TAT)



Multiprocessing Environment

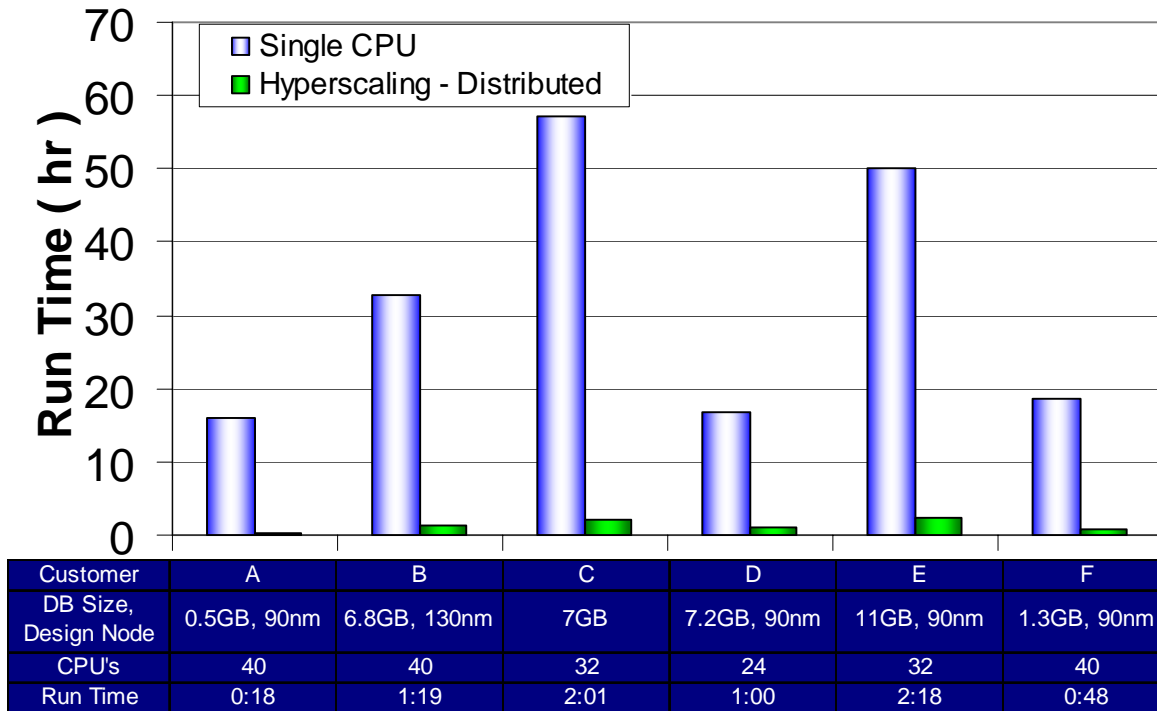


Calibre nmDRC Performance Improvement

- Hyperscaling provides a dramatic speed up

- Excellent scaling over a range of job sizes and types

Single CPU vs. Hyperscaling - Distributed



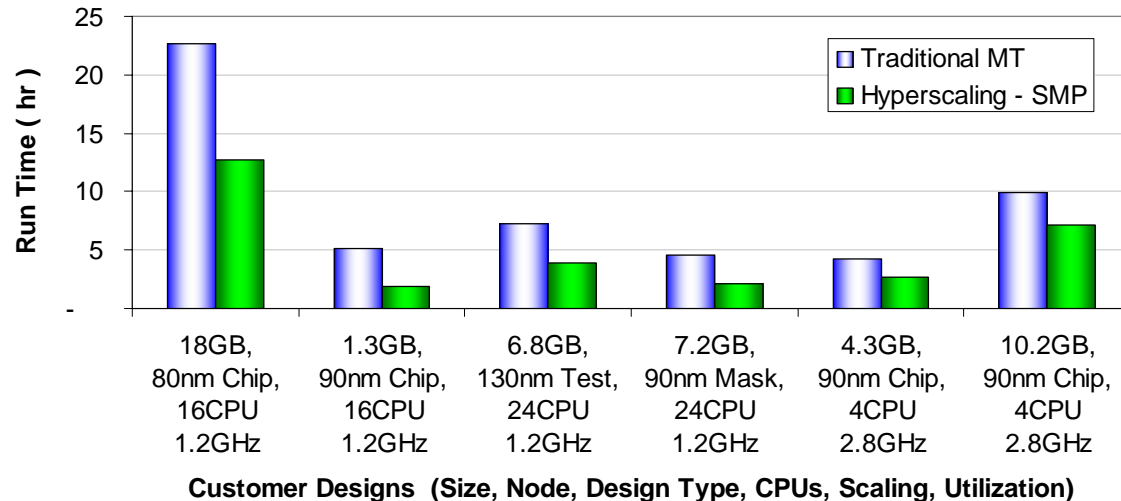
Calibre nmDRC

Performance Improvement - SMP

- **Hyperscaling delivers improved TAT on existing CAPEX**

- **Extends life**
- **Supports a wide range of H/W platforms**
- **Does not *require* H/W investment**

Traditional MT (SMP) vs. HyperScaling (SMP)



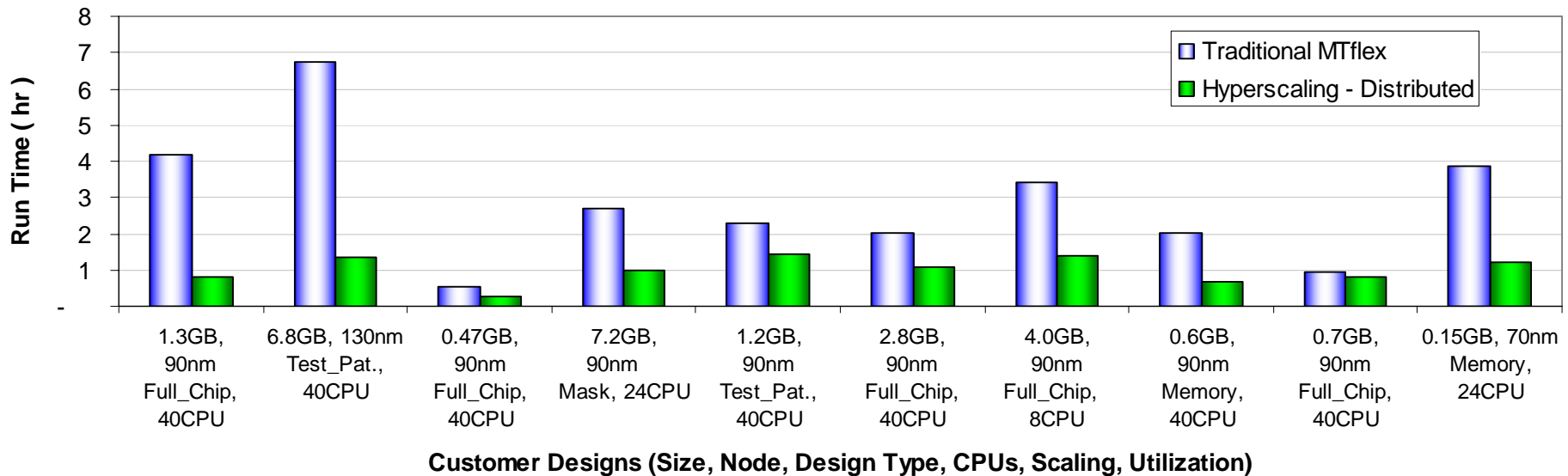
- **Average improvement 1.9x**

Calibre nmDRC

Performance Improvement - Distributed

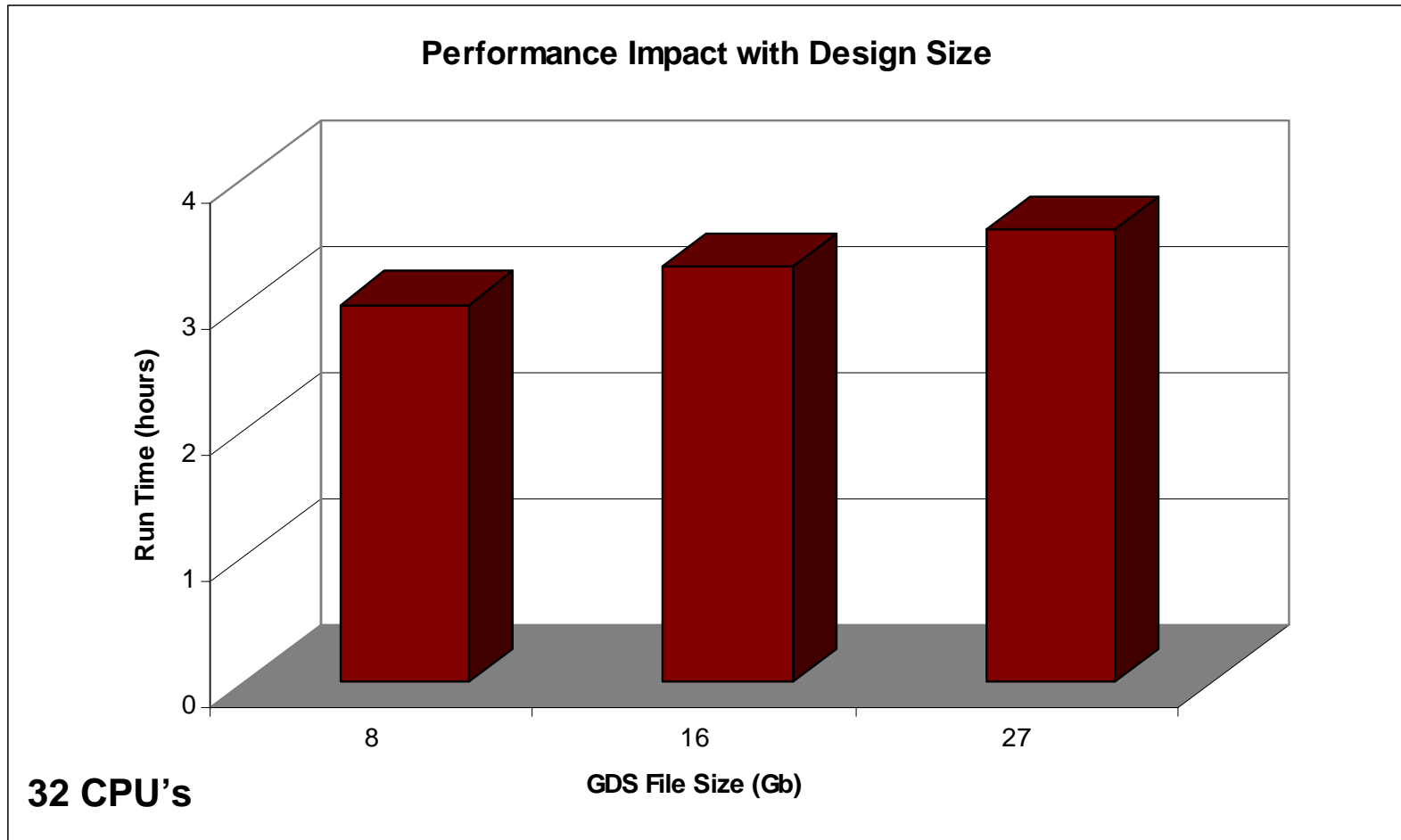
- **Hyperscaling provides fast TAT on distributed hardware**

Traditional Mtflex (Distributed) vs. Hyperscaling (Distributed)



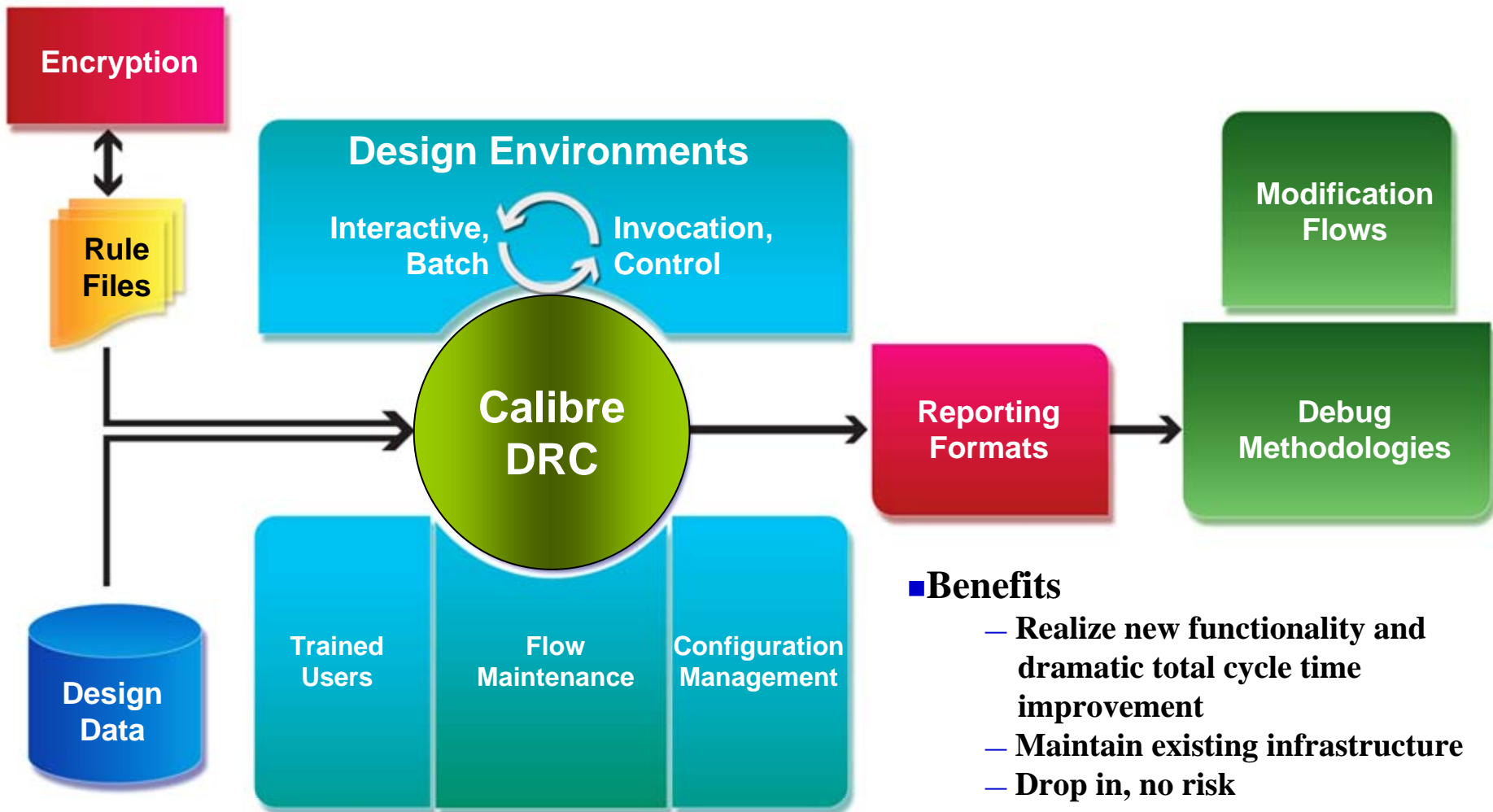
- **Average improvement 2.9x**
- **4 longest designs improved by 3.8x**

Performance Scaling with Design Size



Performance insensitive to data volume

Calibre nmDRC: Drops Into Current CAD Environment Without Disruption



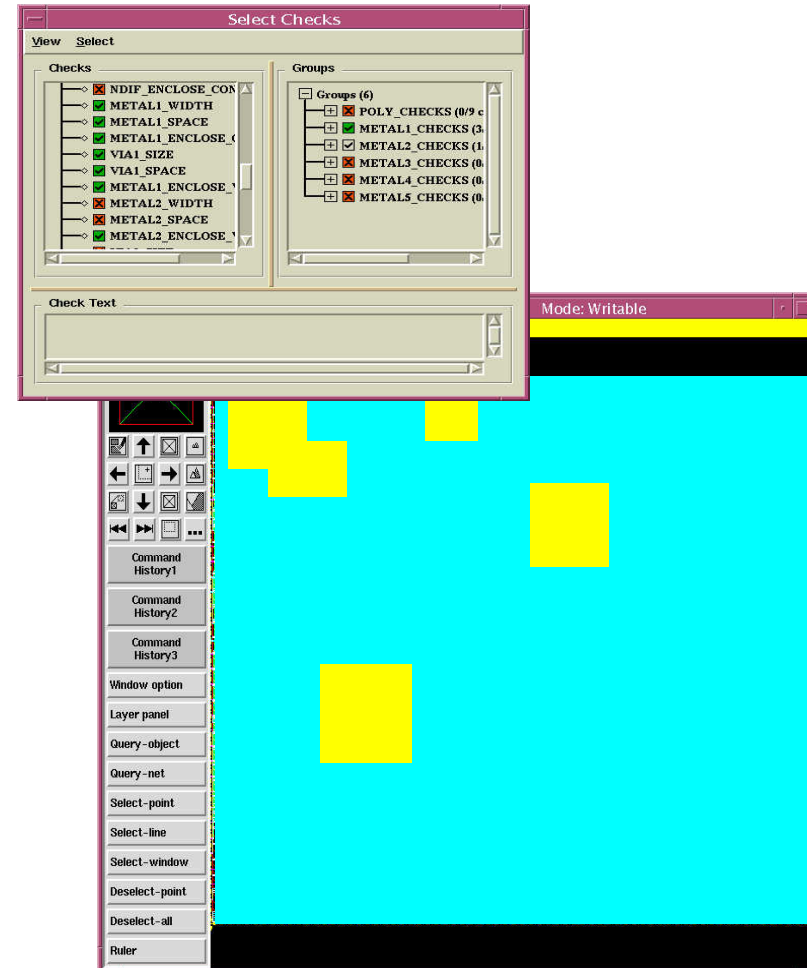
■ Benefits

- Realize new functionality and dramatic total cycle time improvement
- Maintain existing infrastructure
- Drop in, no risk

Calibre nmDRC

Dramatically Reduced Iteration Runtimes

- **Incremental DRC**
 - **Highlight errors as identified**
 - **Begin debug immediately - before job completion**
 - **Automatically identify changed regions**
 - **DB Diff**
 - **Minimize subsequent runtimes**
 - **Stream-out only changed areas**
 - **Run only affected checks**



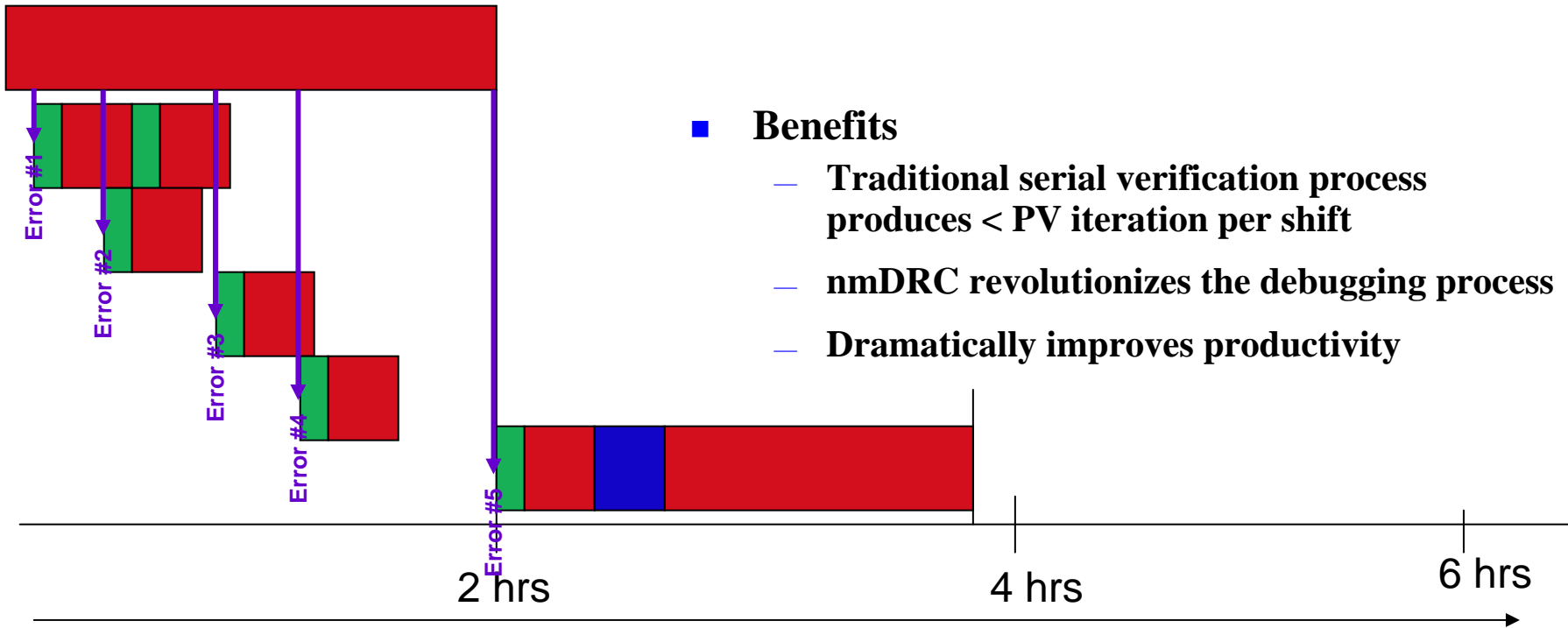
Calibre nmDRC

Dramatically Reduced Iteration Runtimes

Traditional Serial DRC Verification



Calibre nmDRC: Dynamic Results Visualization and Incremental Verification



■ Benefits

- Traditional serial verification process produces < PV iteration per shift
- nmDRC revolutionizes the debugging process
- Dramatically improves productivity

Calibre nmDRC

Modern Development Tools

Traditional SVRF Recommended Rule Metal1

```
METALL1.1R#rfa#b0.28 = INT ame1 >=0.256 <0.28 ABUT >0<90 OPPOSITE REGION
METALL1.1R#rfa#b0.30 = INT ame1 >=0.28 <0.30 ABUT >0<90 OPPOSITE REGION
METALL1.1R#rfa#b0.32 = INT ame1 >=0.30 <0.32 ABUT >0<90 OPPOSITE REGION
METALL1.1R#rfa#b0.28 (@ (Minimum METAL1 width >=0.256<0.28)
DFM ANALYZE METALL1.1R#rfa#b0.28 METALL1.1R#rfa#b0.30 METALL1.1R#rfa#b0.32 >=0
[(COUNT(METALL1.1R#rfa#b0.28))*1.0/AREA()]
RDB ONLY "yield.rdb"
}
METALL1.1R#rfa#b0.28 c (@ output RR yield prediction to RDB BY CELL
@ check: METALL1.1R#rfa
DFM ANALYZE METALL1.1R#rfa#b0.28 METALL1.1R#rfa#b0.30 METALL1.1R#rfa#b0.32 >= 0 BY CELL NOPSEUDO
[(COUNT(METALL1.1R#rfa#b0.28))*1.0/AREA()]
RDB ONLY "yield.rdb"
}
METALL1.1R#rfa#b0.28 (@ (Minimum METAL1 width >=0.256<0.28)
COPY METALL1.1R#rfa#b0.28
}
METALL1.1R#rfa#b0.30 (@ (Minimum METAL1 width >=0.28<0.30)
DFM ANALYZE METALL1.1R#rfa#b0.28 METALL1.1R#rfa#b0.30 METALL1.1R#rfa#b0.32 >=0
[(COUNT(METALL1.1R#rfa#b0.30))*0.8/AREA()]
RDB ONLY "yield.rdb"
}
METALL1.1R#rfa#b0.30 c (@ output RR yield prediction to RDB BY CELL
@ check: METALL1.1R#rfa
DFM ANALYZE METALL1.1R#rfa#b0.28 METALL1.1R#rfa#b0.30 METALL1.1R#rfa#b0.32 >= 0 BY CELL NOPSEUDO
[(COUNT(METALL1.1R#rfa#b0.30))*0.8/AREA()]
RDB ONLY "yield.rdb"
}
METALL1.1R#rfa#b0.30 (@ (Minimum METAL1 width >=0.28<0.30)
COPY METALL1.1R#rfa#b0.30
}
METALL1.1R#rfa#b0.32 (@ (Minimum METAL1 width >=0.30<0.32)
DFM ANALYZE METALL1.1R#rfa#b0.28 METALL1.1R#rfa#b0.30 METALL1.1R#rfa#b0.32 >=0
[(COUNT(METALL1.1R#rfa#b0.32))*0.6/AREA()]
RDB ONLY "yield.rdb"
}
METALL1.1R#rfa#b0.32 c (@ output RR yield prediction to RDB BY CELL
@ check: METALL1.1R#rfa
DFM ANALYZE METALL1.1R#rfa#b0.28 METALL1.1R#rfa#b0.30 METALL1.1R#rfa#b0.32 >= 0 BY CELL NOPSEUDO
[(COUNT(METALL1.1R#rfa#b0.32))*0.6/AREA()]
RDB ONLY "yield.rdb"
}
METALL1.1R#rfa#b0.32 (@ (Minimum METAL1 width >=0.30<0.32)
COPY METALL1.1R#rfa#b0.32
}
METALL1.1R#rfa# (@ (Minimum METAL1 width)
DFM ANALYZE METALL1.1R#rfa#b0.28 METALL1.1R#rfa#b0.30 METALL1.1R#rfa#b0.32 >=0
[(COUNT(METALL1.1R#rfa#b0.28))*1.0+(COUNT(METALL1.1R#rfa#b0.30))*0.8+(COUNT(METALL1.1R#rfa#b0.32))*0.6]/AREA()]
RDB ONLY "yield.rdb"
}
METALL1.1R#rfa#_c (@ output RR yield prediction to RDB BY CELL
@ check: METALL1.1R#rfa
DFM ANALYZE METALL1.1R#rfa#b0.28 METALL1.1R#rfa#b0.30 METALL1.1R#rfa#b0.32 >= 0 BY CELL NOPSEUDO
[(COUNT(METALL1.1R#rfa#b0.28))*1.0+(COUNT(METALL1.1R#rfa#b0.30))*0.8+(COUNT(METALL1.1R#rfa#b0.32))*0.6]/AREA()]
RDB ONLY "yield.rdb"
}
```

Repeat For Metal2 through Metal9
Total Lines of SVRF Code = 509

Calibre TVF

Recommended Rule Metal1

```
set met111_bin (SLIST 0.256 0.28 0.30 0.32)
Create_RRA_SVRF METALL1.1R (WID_MIN_L1 {ame1 ORTHO} "Minimum METAL1 width") {
$met111_bin (DLIST 1.0 0.8 0.6) {USER $lambda/AREA()}}
```

Call Template = 2 lines of TVF Code

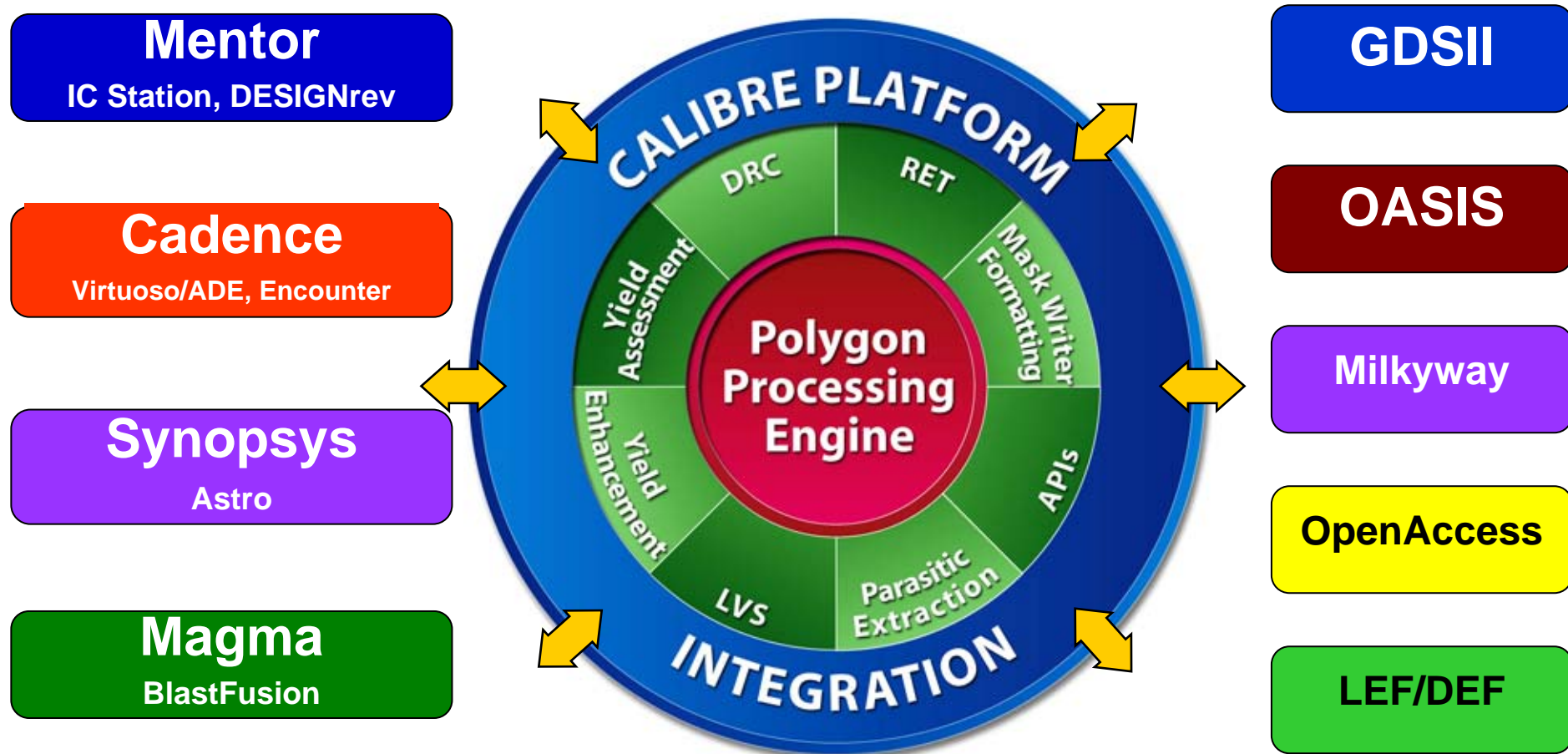
Library Template = 59 lines of TVF Code

Forloop all metals = 3 lines of TVF Code

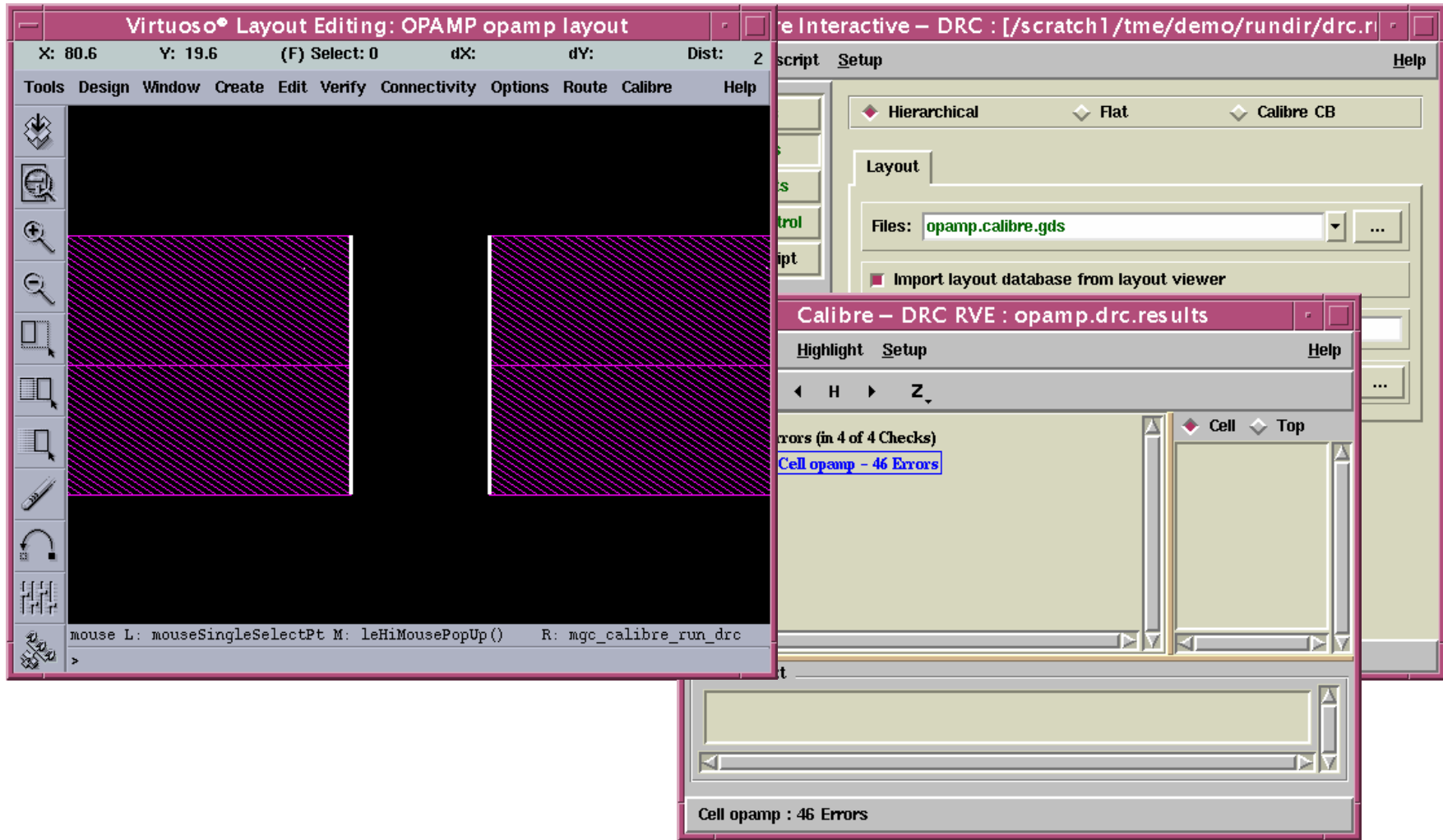
Total lines of TVF Code = 64

- High level programming language
- Simplifies the development and maintenance of advanced rule files

Calibre Integrated into Design Platforms



Virtuoso Integration Example



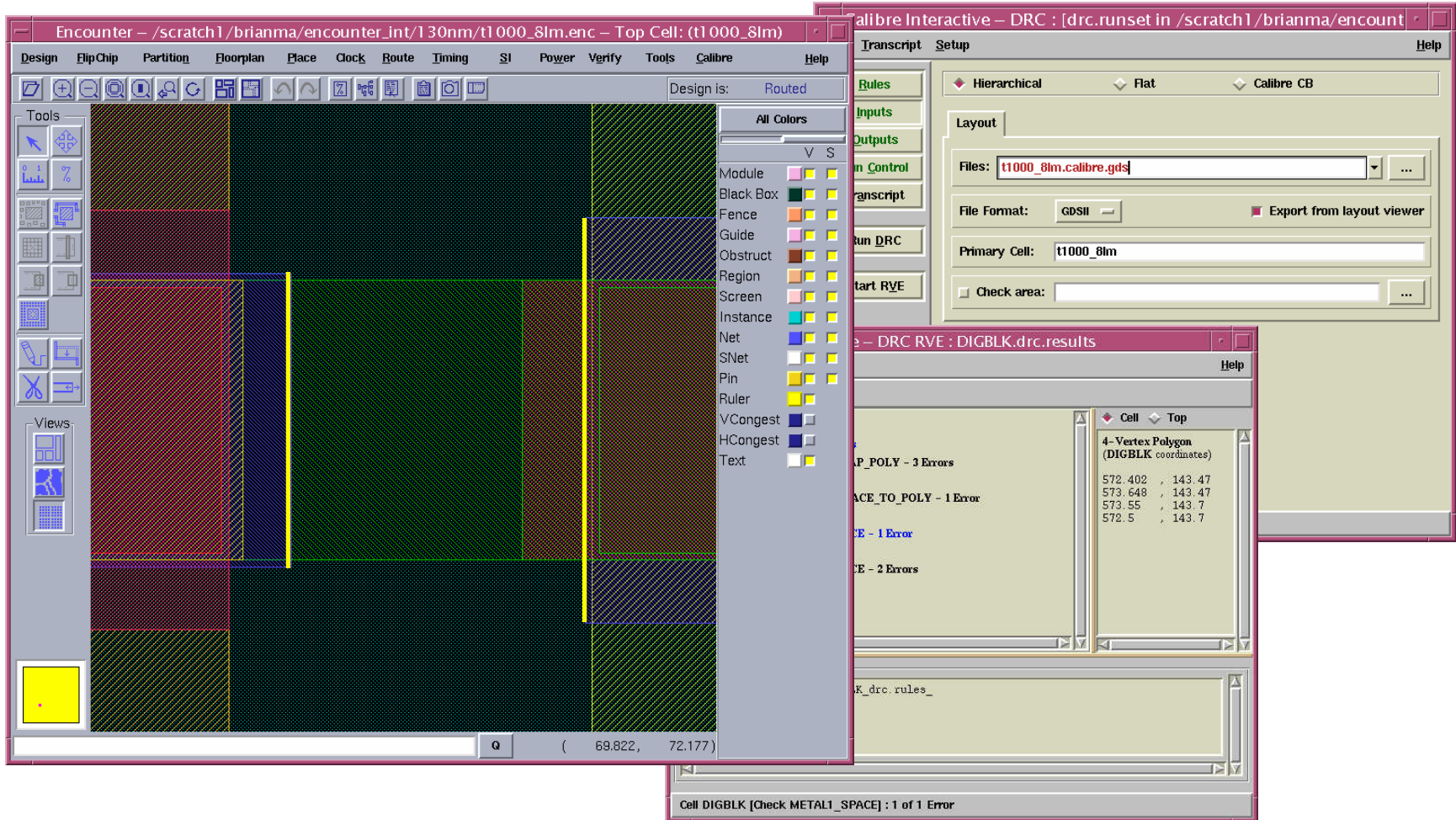
BlastFusion Integration Example

The image displays three windows from the Magma Design Automation software interface:

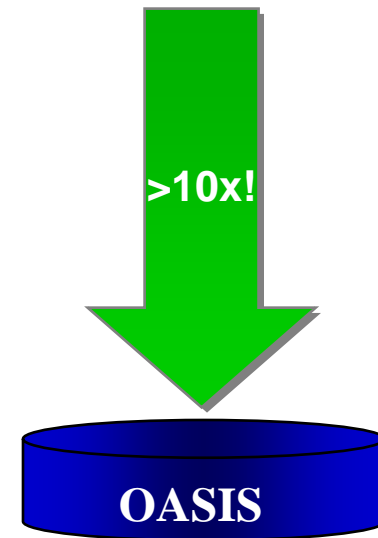
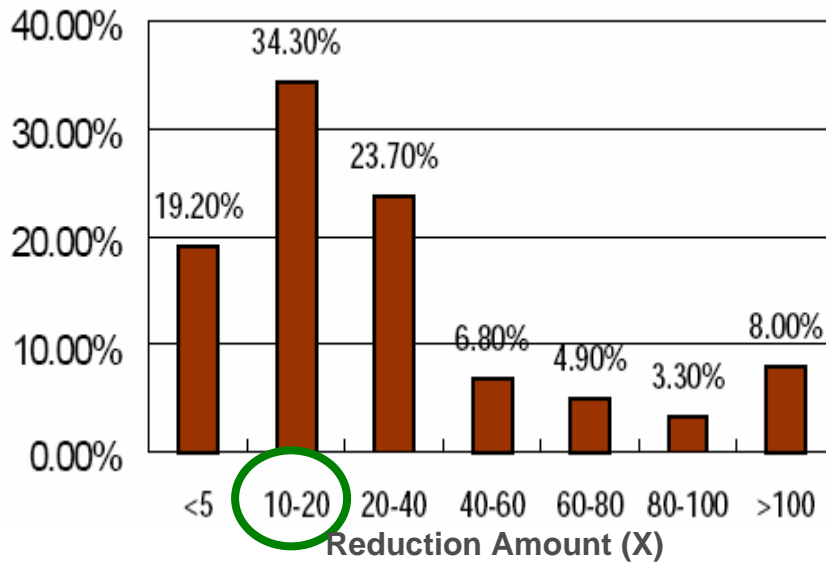
- Calibre – LVS RVE : svdb (opamp)**: Shows a list of discrepancies. The "LVS Results: Designs Don't Match" section is expanded to show "opamp / opamp - 6 Discrepancies", which includes "Incorrect Nets - 1 Discrepancy" (highlighted as "Discrepancy #1") and "Incorrect Ports - 5 Discrepancies".
- Layout - Magma Design Automation**: Shows a detailed physical layout of the circuit, with various components and routing paths visible in different colors.
- schem_12 - Magma Design Automation**: Shows a schematic diagram of a buffer chain. It consists of three inverters labeled BH1_BUF344, BH1_BUF343, and BH1_BUF342, connected in series.

At the bottom of the interface, there are status bars with the text "elect. SHIFT to select multiple. CTR x:221.42u y:107.97u Current Mode: Select Selected: 0" and "Show Messages" buttons.

Encounter Integration Example



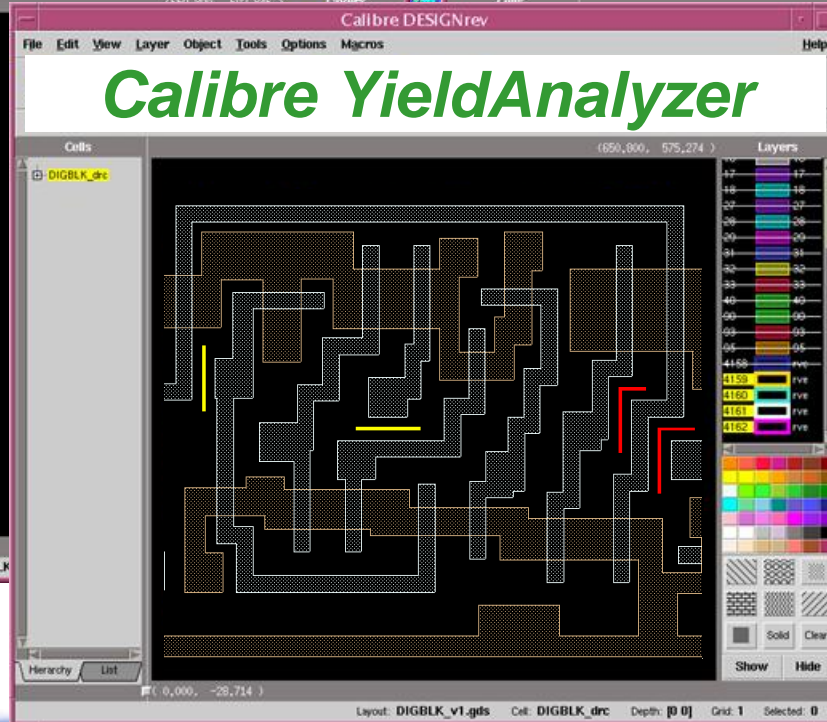
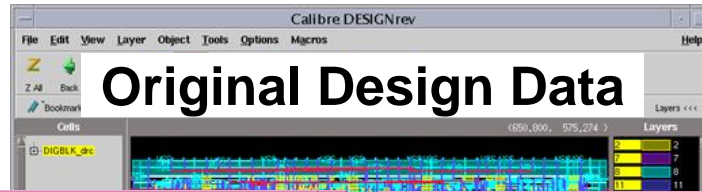
OASIS: Tackling the Capacity Bottlenecks



**Original GDSII-to-OASIS
File Size Reduction Distribution**

Evaluation of 5000 customer GDSII vs OASIS data files!

Statistical Analysis Augments Simple Error Markers



Yield Analysis and Visualization

YRC Rule Summary Table

File View Highlight Tools Setup

Results Properties Tables

Rule Summary Cell Summary Rule/Cell Details

Export Hide

Chip Level Checks by Rule

Type	Check Name	Total	Bin 1	Bin 2	Bin 3	Bin 4
caa	POLY1.SHORT	1.359170	0.0009	0.853859	0.144899	0.860305
rra	LPO2OD	0.418350	0.2564			
caa	POLYCONT.OPEN	0.045529	0.0001			0.028116

Rule Bar Chart

- By Rule Bar Chart
- By Window Color Map
- By Window Histogram
- By Cell Drill Down Report
- By Cell Drill Down Chart

Cell Bar Chart (Single Impact)

Calibre - DRC RVE : cell.rdb

File View Highlight Tools Setup

Results Properties Tables Histograms

Rule Summary Cell Summary Rule/Cell Details

Export Hide

Chip Level Checks by Cell by Rule

Type	Check Name	Cell Name	Total	Bin 1	Bin 2	Bin 3	Bin 4
caa	POLY1.SHORT	DIFFRHQX1	4.561810	0.003672	0.236091	1.993580	2.72
caa	POLY1.SHORT	DIFFRX1	4.405070	0.004271	0.232527	1.593770	2.60
caa	POLY1.SHORT	DIFFRX2	4.110290	0.003356	0.171188	1.380900	2.55
caa	POLY1.SHORT	DIFFRX4	4.009010	0.003333	0.165086	1.359980	2.48
caa	POLY1.SHORT	DIFFSX1	3.904480	0.003316	0.190746	1.340810	2.36
caa	POLY1.SHORT	NOR4BX1	3.637090	0.002966	0.150101	1.254330	2.22
caa	POLY1.SHORT	NAND4X1	3.526520	0.001167	0.092680	1.228200	2.20
caa	POLY1.SHORT	AOI31X1	3.479800	0.002125	0.119083	1.197670	2.16
caa	POLY1.SHORT	NAND4BXL	3.411570	0.002193	0.163513	1.179960	2.08
caa	POLY1.SHORT	AOI221X1	3.391300	0.004053	0.159914	1.167130	2.05
caa	POLY1.SHORT	AOI222X1	3.345290	0.001972	0.114480	1.117300	2.11
caa	POLY1.SHORT	AOI33X1	3.331980	0.001041	0.095484	1.086570	2.16

Output Colormap for Result POLY1.SHORT#caa#c<1>

Calibre - DRC RVE : cell.rdb

File View Highlight Tools Setup

Results Properties Tables Histograms

(1) DV

top + POLY1.SHORT#caa#c<1> (DV Range: 0 - 4.56181, Total 73)

Output Colormap for Result POLY1.SHORT#caa#c<1>

Model Based Verification: From DRC to nmDRC

Random

Systematic

Parametric

Rule Based

Calibre YieldAnalyzer Recommended Rule Analysis

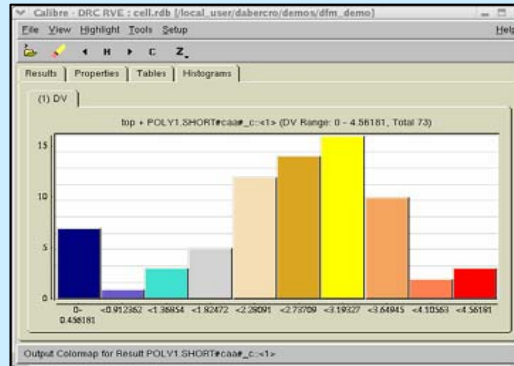
Rule Summary | Cell Summary | Rule/Cell Details

Export Hide Total : 10.954883

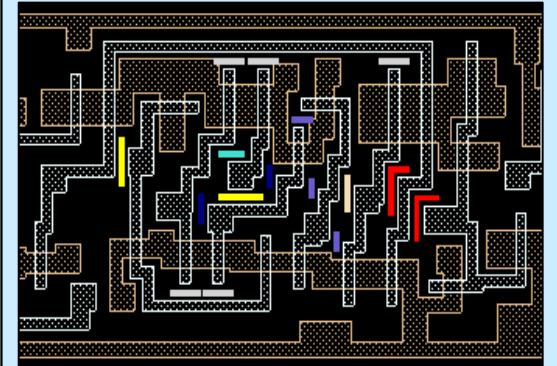
Chip Level Checks by Rule

Type	Check Name	Total	Bin 1	Bin 2	Bin 3	Bin 4
caa	V1_OPEN	4.39831	0.000381	0.102517	1.179410	3.116000
rra	V1Redun	3.56141	3.554630	0.006777	0.000000	
caa	POLY1.SHORT	1.65461	0.001173	0.067386	0.534559	1.051490
rra	LPO2OD	0.452448	0.284920	0.162340	0.005187	
rra	M1EncV1	0.36205	0.000000	0.293605	0.035410	0.030035
caa	M1.SHORT	0.259417	0.003007	0.032531	0.106567	0.117312
rra	M1LEXV1	0.155394	0.000000	0.153985	0.002009	
caa	POLYCONT.OPEN	0.0890792	0.000205	0.004391	0.027519	0.056963
rra	M1MinArea	0.0212342	0.003887	0.015366	0.001744	0.000238
rra	CNET.V1Redun	0.000194335	0.000194	0.000000	0.000000	
rra	CNET.LPO2OD	0.000135814	0.000119	0.000013	0.000003	

Calibre YieldAnalyzer Recommended Rule Analysis

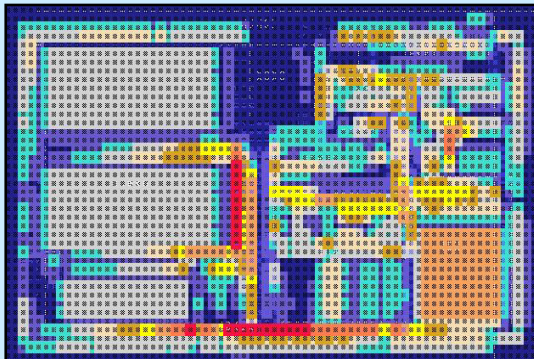


Calibre YieldAnalyzer Recommended Rule Analysis

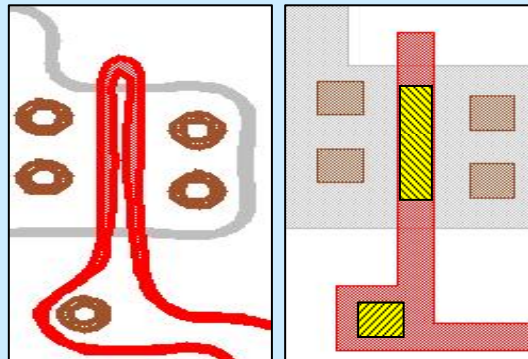


Model Based

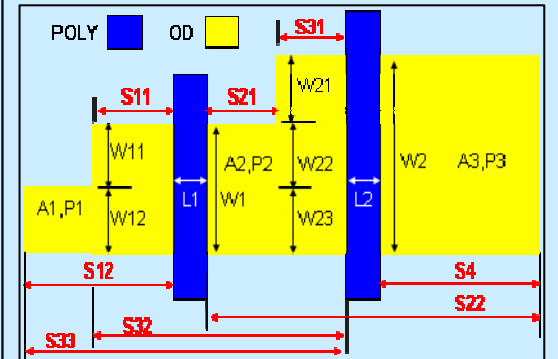
Calibre YieldAnalyzer Critical Area Analysis



Calibre LFD Litho Variation Analysis



Calibre LVS/xRC/xL Mfg Aware Silicon Modeling

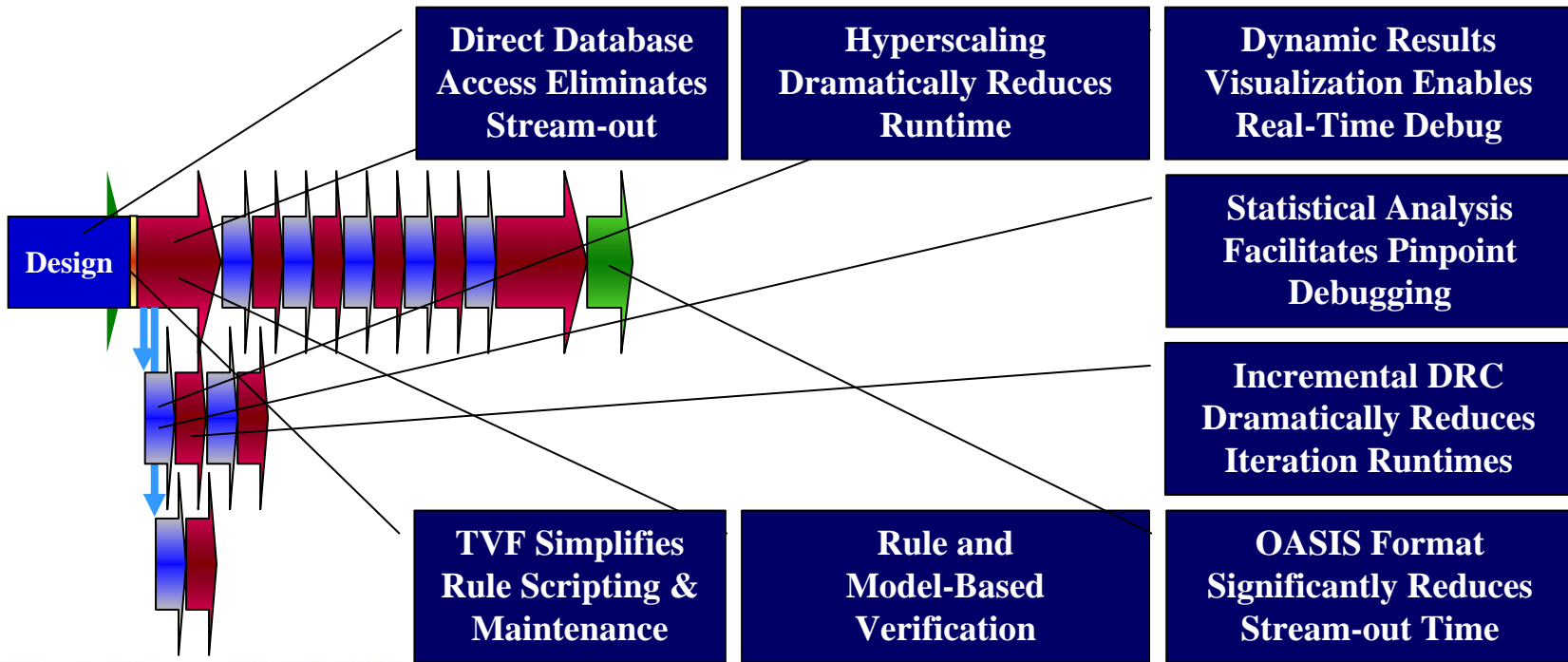


Solving the WHOLE Cycle Time Issue

Classic Serial Verification



nmDRC Verification



Summary

- **The Calibre nm Platform provides the industry's most robust platform for design to silicon in the DFM era**
- **With Calibre nmDRC we continue to provide best in class performance, improved total TAT and the design database integration required for nanometer design**

Mentor Graphics®

www.mentor.com

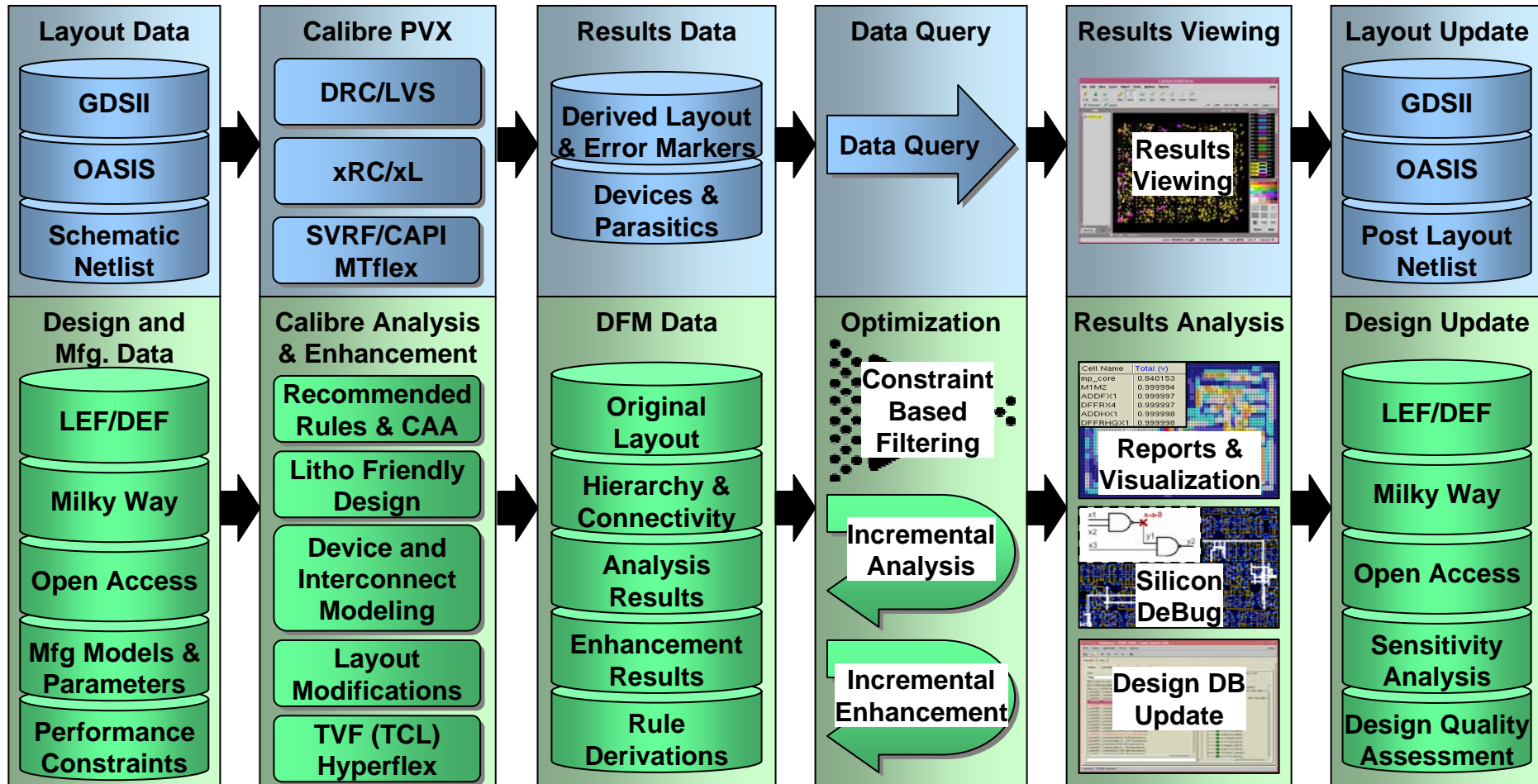
Design Environment Integration: How It Works

The image displays the Calibre Design Environment (DRC RVE) interface for the cell DIGBLK. The main window, titled "Calibre - DRC RVE : DIGBLK.drc.results", shows a hierarchical error report:

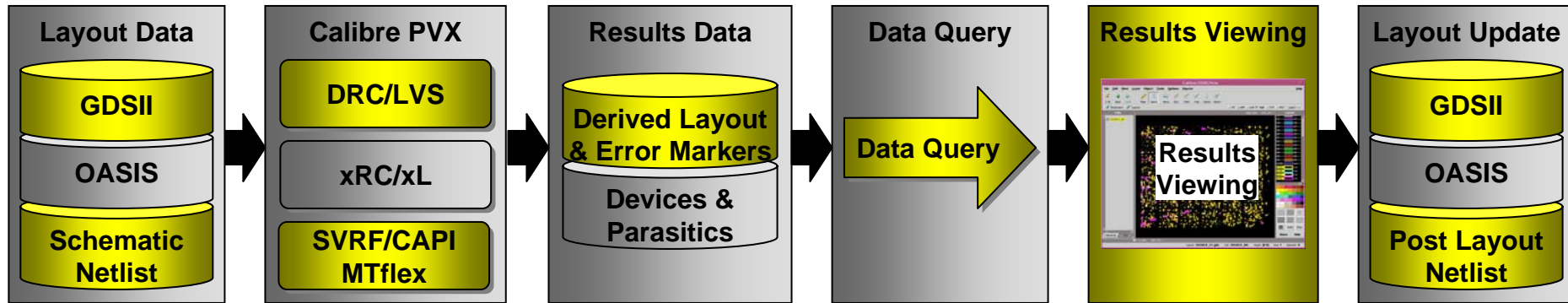
- 7 Errors (in 4 of 55 Checks)
 - Cell DIGBLK - 7 Errors
 - Check PDIF_OVERLAP_POLY - 3 Errors
 - 01 02 03
 - Check CONTACT_SPACE_TO_POLY - 1 Error
 - 01
 - Check METAL1_SPACE - 1 Error
 - 01
 - Check METAL2...

The "Checktext" window displays the rule details: "Rule File Pathname: ..." and "Min Metal 1 space = 0.". The layout view on the right shows a cross-section of the design with a yellow trapezoidal shape highlighted. The "Calibre Interactive - DRC : [DIGBLK]" window in the foreground shows the "Setup" tab with "Files: DIGBLK.gds" and "Primary Cell: DIGBLK". The background window shows the "demo" menu with options like "Run DRC ...", "Run LVS ...", and "Run PEX ...".

Introducing the New Calibre nm Platform

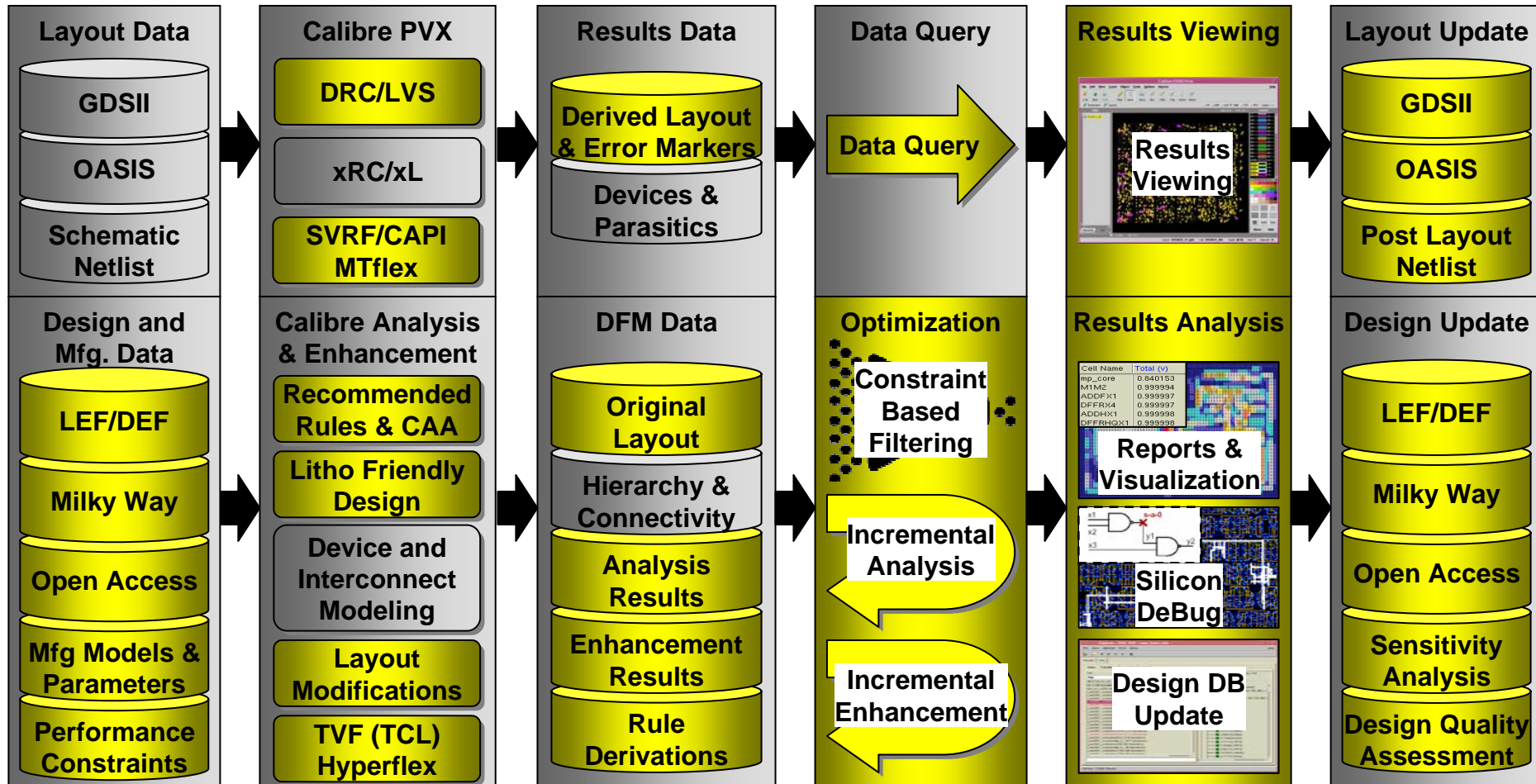


Traditional DRC

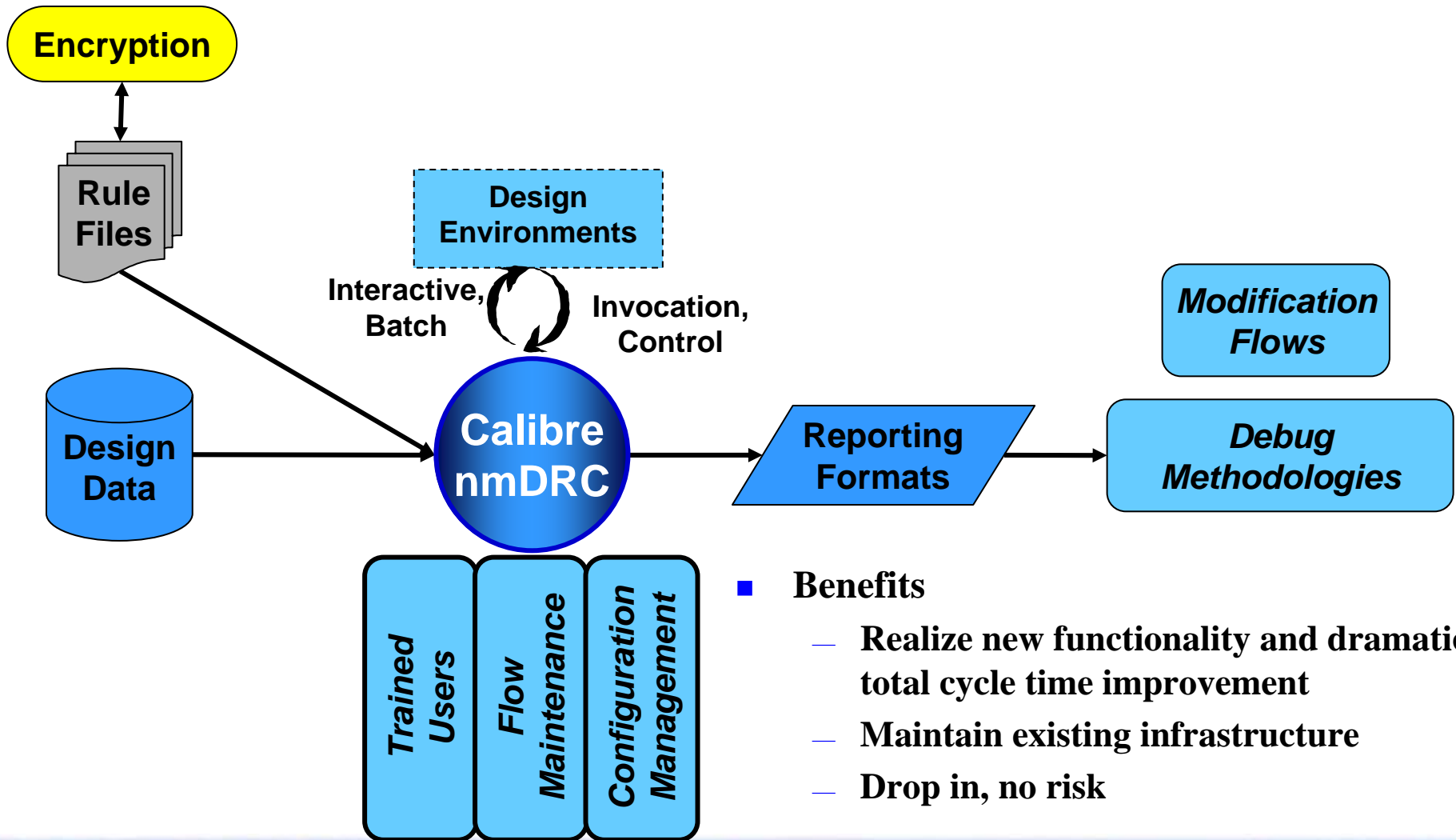


Introducing Next Generation DRC

Calibre nmDRC



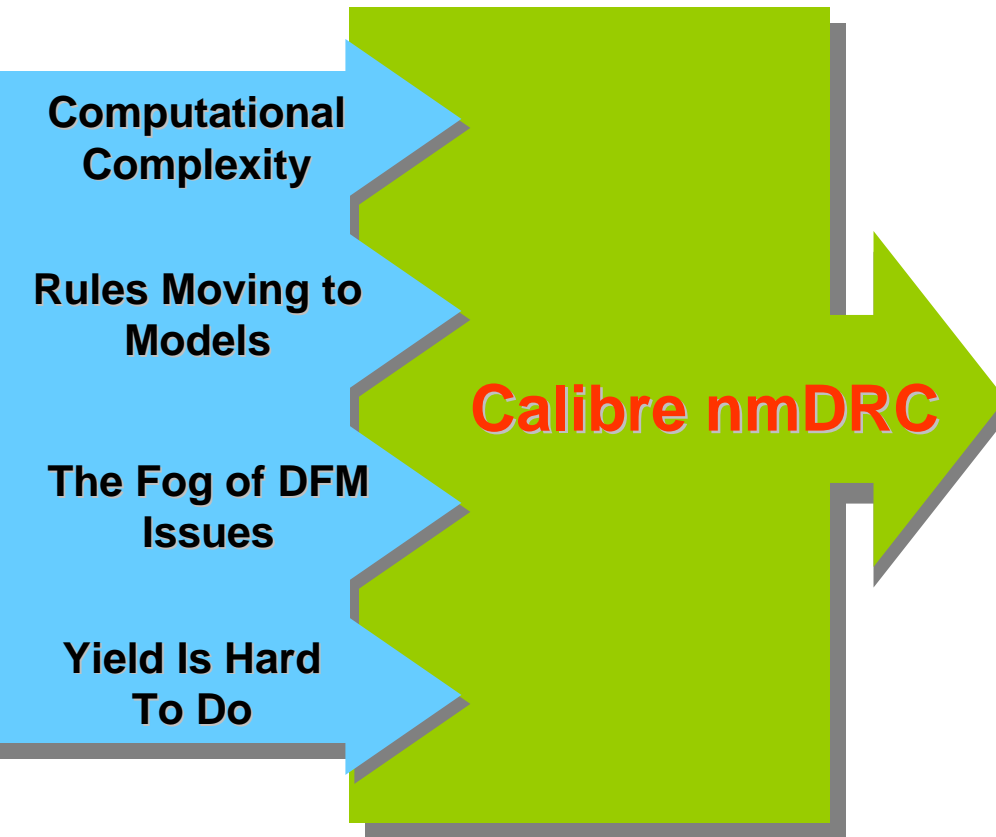
Calibre nmDRC: Drops Into Current CAD Environment Without Disruption



■ Benefits

- Realize new functionality and dramatic total cycle time improvement
- Maintain existing infrastructure
- Drop in, no risk

Advantages of Calibre nmDRC



- **Faster Turn Around Time**
- **Modern Development Tools**
- **Model-Based Verification**
- **Statistical Analysis to Augment Simple Error Markers**
- **Integration that allows tight 'fix' loops**
- **Higher productivity**