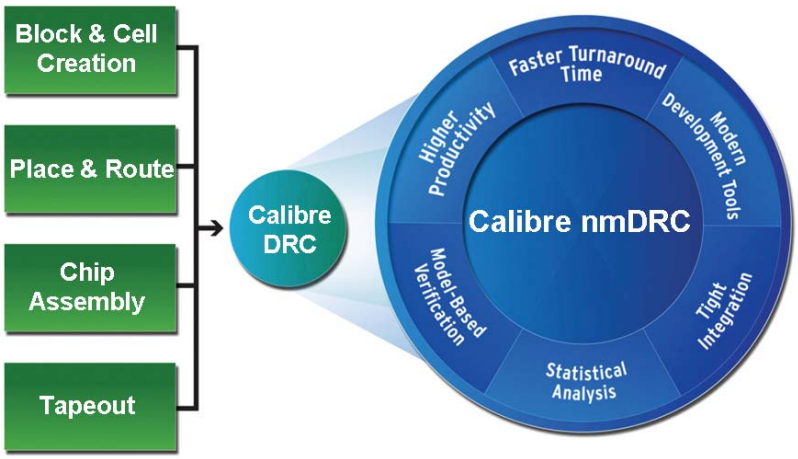
Calibre nmDRC

D A T A S H E E T



DRC has changed from the traditional pass/no pass compliance check to a comprehensive methodology that supports multiple analyses, increased performance and scaling, enhanced productivity, and improved cycle times.

Evolution of the Calibre Architecture

The Calibre® core processing engine continually evolves to meet the demands of shrinking geometries and complex manufacturing methodologies. While traditional DRC methods of pass/no pass have served well for many years, simple compliance is no longer adequate to account for the variety and complexity of situations that occur in nanometer era processes.

To ensure high yields in nanometer process technologies, designers require new information and new levels of judgment that go beyond design rule checking to include statistical yield analysis. They need new ways to assess the quality of their designs in light of the more complex process constraints and larger process variations they now face.

Mentor Graphics has built upon the industry's production-leading Calibre architecture to create the 5th generation Calibre processing engine. **Calibre nm** advances the core technology to give designers comprehensive analysis capabilities, and faster run and cycle times. Through advanced DRC methods, scaling, performance and analysis, designers will be able to manage the handoff to manufacturing in ways that result in a whole new level of productivity.

Key Product Benefits

- **Comprehensive sign-off for nanometer designs,** accounting for both compliance and model-based physical verification.
- **Hyperscaling significantly improves runtimes and productivity gains,** and offers advanced data processing options that make efficient use of existing multi-core and distributed processing farms, and extends the useful life of existing capital equipment.
- **Model-based verification enables comprehensive failure analysis in a single robust environment** to determine location of the most significant yield improvement opportunities. Yield metrics are graded by issue, cell and window within the layout tool.
- **Incremental verification** allows designers to begin debugging within seconds rather than hours. "Real time" debugging reduces overall iteration and cycle time, making efficient use of the designer's time.
- **Direct database read/write access** provides back annotation of DFM data into design databases, including GDSII, OASIS, LEF/DEF, MilkyWay and OpenAccess. The OASIS stream file format reduces file size for faster read/write, facilitates file transfer and data storage.
- **Calibre TVF rule file support** significantly reduces code input, simplifying the development and maintenance of advanced rule files..

Calibre nm Hyperscaling for Dramatic Runtime Improvement

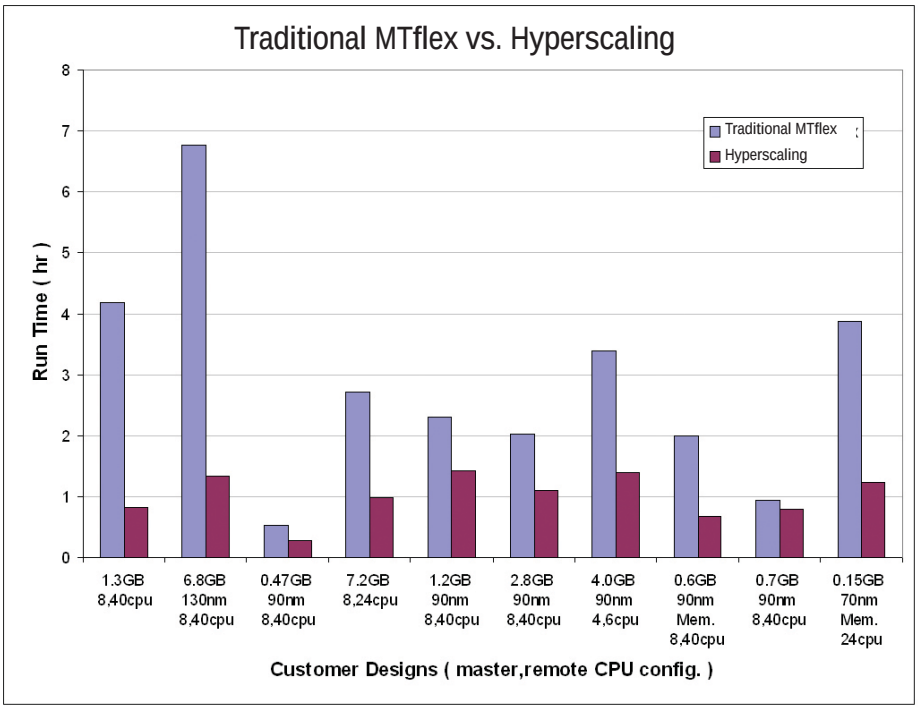
With increasing size and complexity of designs, and the explosion of new rule checks required for the next technology node, the need for faster turn-around-time (TAT) is critical.

Calibre nm Hyperscaling extends Calibre's production-proven performance architecture to significantly increase scaling and reduce TAT. Calibre Hyperscaling runs in either central or distributed shared memory processor environments, such as 8-way Opteron or EM64T Linux boxes. Allowing continued use of existing equipment saves design teams additional capital expenditures.

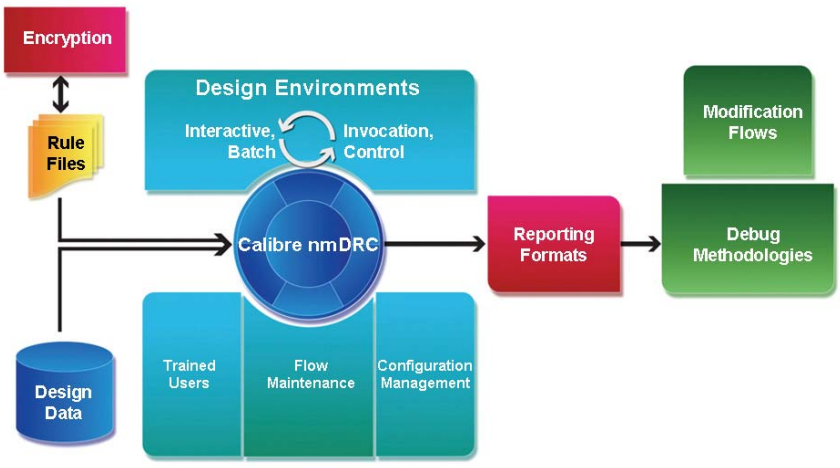
Design verification is completed faster with existing hardware or can be further improved on new hardware, and fewer hardware resources are required. Cell block verification jobs can be run in parallel as multiple designers work to complete subsections of a design on the same hardware, which is tied together for full chip verification. Performance and TAT goals can be achieved or exceeded at a fraction of normal cost.

Hyperscaling also provides productivity improvements with no changes to current SVRF decks, protecting investments in deck development and staff expertise. SVRF decks created years ago, as well as the most advanced 45nm decks, run faster.

Calibre nmDRC Hyperscaling improves performance whether designers are working in 180nm designs or 45nm designs.



Calibre's new architecture enables a "hyperscaling" mode that improves scaling to as much as 40X on existing equipment and continues scaling out to 100 CPUs. Even on 8 CPUs, DRC runs have improved from 5x scalability to 8x. On 24-CPU machines, the scalability is still nearly linear, up to 23x. In the graphic above based on customer benchmarks of Calibre MTflex vs Calibre nmDRC with Hyperscaling, Hyperscaling has dramatic productivity gains, with 2X and greater runtime improvement.

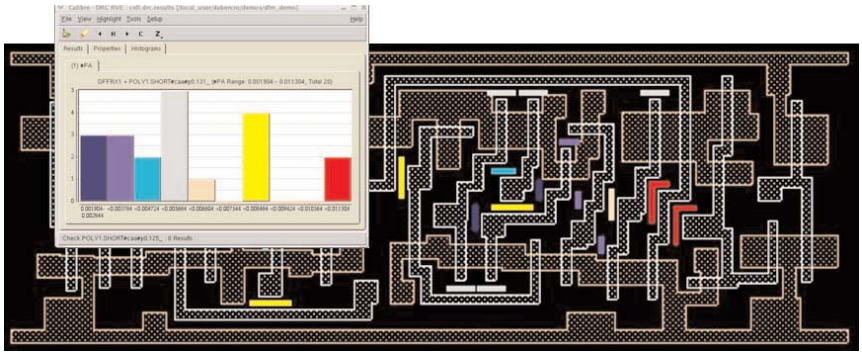


Calibre nmDRC drops into the designer's current CAD environment without disruption or risk. Users can immediately realize new functionality and dramatic total cycle time improvement within existing infrastructure.

Model-Based Verification for Critical Failure Analysis

Calibre nm brings a new, more comprehensive methodology to sign-off. Model based verification offers designers a single robust environment that facilitates the analysis of both critical area and recommended rules. These capabilities address the key sources of yield loss: random and systematic design flaws. Designers can visualize the results of this model using graphical displays and data-driven tables to easily show how and where time should be spent to improve yield. This is done in the form of a Calibre design-for-manufacturing (DFM) deck, giving designers a natural transition from a 'golden' DRC deck to a 'golden' DFM deck.

Calibre nm extends the DRC SVRF language to provide manufacturing teams a method in which to communicate yield and yield modeling information to the designer. It determines the location of the most significant yield improvement opportunities, providing graded yield metrics by issue, cell, window, etc. Calibre nm assesses the weighted "greyscale" of features that fail to meet recommended rules, and assesses the weighted sensitivity to random particles using critical area analysis. It evaluates both in the same run deck and reviewing environment, giving the designer a format in which to understand trade-offs between the two analyses and to make decisions about enhancing the layout for yield improvement. Designers can focus on the flaws that will have the most impact, which improves both productivity and yield.



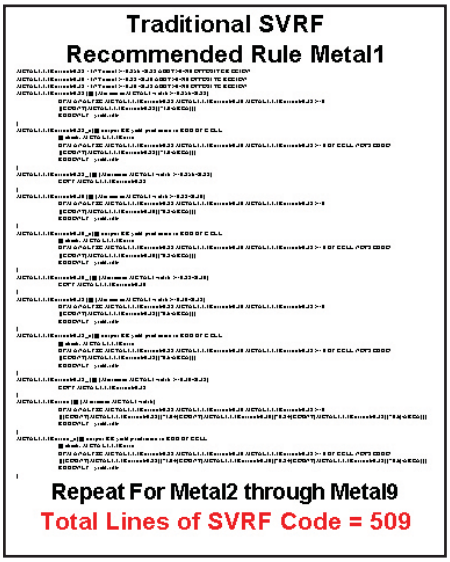
Calibre prioritizes critical area and recommended rule violations, combining the checks in a single viewing environment for analysis. This gives designers a full picture in which to understand design/yield tradeoffs and make informed choices.

Database Direct Read

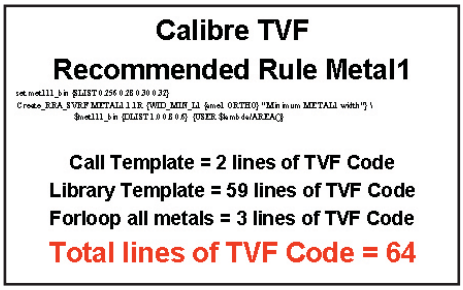
Calibre is unique in that it reads all open data formats, including GDSII, OpenAccess, Milkyway, LEF/DEF, and OASIS. A single set of operations can be translated for all design environments, including different versions of software. The direct read function also eliminates the GDS stream out. Easily integrated into third party tools, the database interface automates layer mapping, backannotates DFM optimizations into the design database, and no longer requires significant disk space for holding the GDSII data for every iteration, thereby saving disk space. No additional layout tool is required for direct read.

TVF

Tcl Verification Format (TVF) is a high-level, SVRF language preprocesor that drastically reduces the number of lines of code needed to execute a DRC run. This simplifies rule scripting and maintenance, and the need to change and validate every line of code. It supports Boolean expressions, conditional and looping flow controls, variables for layer names, procedural encapsulation, and mathematical functions in expressions.



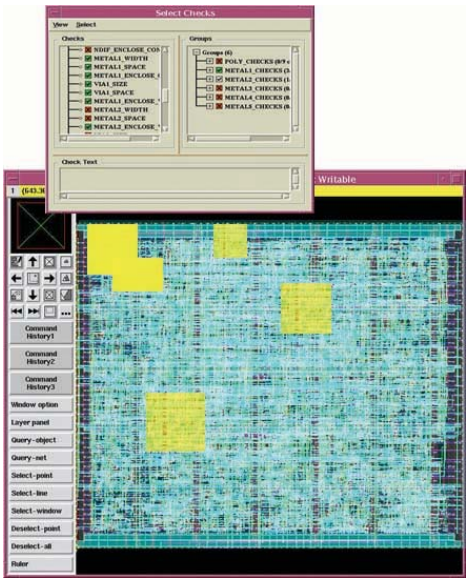
TVF drastically reduces lines of code for DRC runs. In this example of a recommended rule for prioritizing metal line widths, code is reduced from 509 lines of SVRF to just 64 lines of TVF code.



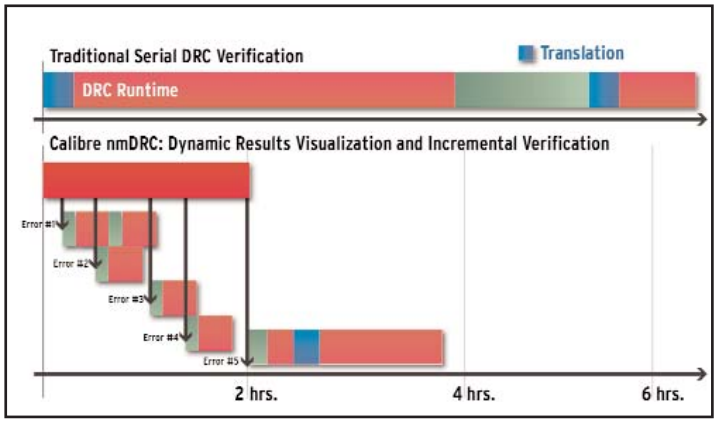
Incremental Verification

Incremental verification fundamentally changes the iteration process. In traditional methods, a designer must wait until the DRC run is completed before beginning the debug process. Incremental verification allows designers to begin debugging immediately during the run time, as soon as the first error is identified.

Calibre nm automatically identifies changed regions (shown in the graphic at right), reads only the changed areas and runs only the effected checks. Calibre nm also eliminates translation time, allowing further reduction of overall cycle time and giving designers the option of performing several run/debug cycles in a single day.



Calibre nmDRC identifies error regions, then reads only the changed areas, dramatically reducing cycle time.



The graphic above illustrates how the iteration cycle is enhanced: The traditional six-hour DRC cycle time permits only one complete cycle in a day. It may afford enough time to get a second debug cycle started, but no more.

Incremental DRC, representative of all Calibre nm improvements (Hyperscaling, Incremental Verification and Direct Database Read), does not require translation, shortens iteration time through concurrent debugging and DRC runs, and improves productivity. The entire physical verification cycle can be completed in less than a day.

The Calibre nm Platform

The industry standard Calibre platform from Mentor Graphics offers a complete solution that bridges design-to- manufacturing. It provides a data communication link crucial to improved yield and reliability in nanometer IC designs. Fueled by a single, powerful polygon processing engine, the Calibre platform includes solutions for physical verification, parasitic extraction, resolution enhancement, mask data prep, litho-friendly design, and design for manufacturing.

Complete Calibre rule files and extensive coverage of the nanometer processes for DRC and DFM are available at a majority of the world's semiconductor foundries, including Chartered, IBM, Jazz Semiconductor, STMicroelectronics, TSMC, and UMC. Calibre is the physical verification standard used internally by Chartered, TSMC and UMC.

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