Litho-Friendly Design: Capturing Process Variability for the Design Flow

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Overview

Traditionally, after the hand-off of a design, it has been the foundry's responsibility to ensure printability. But with process technologies of 90nm and below, the entire design flow is susceptible to yield inhibitors. That's why designers, foundries and EDA toolmakers are turning to design-for-manufacturing (DFM) methodologies that promise improved flows and solutions that manage and analyze nanometer effects.

However, in order for a DFM recommendation to be of value to designers, it must include details about how a particular design will manufacture given the specific process. This requires a tool that can communicate an awareness of the process window at all stages of the design flow. This capability is the key benefit of an advanced DFM technology known as litho-friendly design (LFD), the goal of which is to capture process variability to improve layout robustness.

The Advent of Litho-Friendly Design

With the shrinking geometries and complex manufacturing processes indicative of the nanometer era, gaining acceptable yield on a silicon wafer has become more and more elusive. Unlike the 0.35µm and 0.25µm process nodes when designs could be manufactured as drawn and yield outcomes would stabilize quickly, yield in nanometer nodes has declined sharply and stabilization has been more difficult to attain.

The reason is that as feature sizes get smaller, the dominant cause of defects changes. At larger processes, yield limitation is dominated by random defects. Despite the best clean room efforts, particles still find a way to land on chips or masks, causing shorts or opens. In nanometer processes, the dominant source of yield loss is pattern-dependent effects. These defects are a result of the design's features being smaller than the wavelength of light, the basic element of silicon manufacturing. This shift to pattern-dependent yield issues is forcing a change in the way designers and manufacturers approach their flows.

Traditionally, after the hand-off of a design, it has been the foundry's responsibility to ensure printability. But tweaking a mask is no longer sufficient to ensure image fidelity. With process technologies of 90nm and below, the entire design flow is susceptible to yield issues. As a result, yield issues are becoming more than a foundry and lithographic issue; they will also be a design issue. That's why designers, foundries and EDA toolmakers are turning to design-for-manufacturing (DFM) methodologies that promise improved flows and solutions that manage and analyze nanometer effects.

DFM is not a new concept. Design rule checks (DRC) were the first wave, created to ensure that layout specifications met the requirements of manufacturing through simple yes/no or pass/fail rules. While pass/fail is still a valid verification method, there are many new effects and interdependencies that rules-only verification methods have difficulty capturing. The copper manufacturing process, metal fill, via insertion, and wire spreading, all designed to improve yield, might eventually have a negative effect on yield outcome.

A second wave of early DFM came at the 180nm node when post-tapeout applications such as optical process correction (OPC), phase shift masks (PSM) and other resolution enhancement techniques (RET) were used to modify the design at the foundry in order to ensure printability. At the same time, physical verification also expanded capability to account for issues such as planerization and antenna effects. Although these extensive post-layout modifications resulted

in a layout that was unrecognizable by the designer, the resulting manufactured IC matched the designer's intent.

Now a third wave of change is descending upon the industry, one that embodies a current view of DFM, which supposes that just because a feature is manufacturable doesn't mean that it won't have a negative effect on yield. This trend can be characterized by a move from a simple yes/no hand-off from designer to manufacturer to a less definitive “grey area” of analysis with priorities, rankings and trade-offs. This is bringing a completely new breed of DFM tools that find opportunities to further enhance the design for improved yield, enabling the user to see where the ability and/or inability to modify the layout will have a bearing on yield.

However, in order for a DFM recommendation to be of value to designers, it must include details about how a particular design will manufacture given the specific process. This requires a tool that can communicate an awareness of the process window at all stages of the design flow. With such a capability, every stage of the design flow, and each design team in the flow can be made process and yield aware.

This capability is the key benefit of an advanced DFM technology known as litho-friendly design (LFD). It captures information on process window effects so that designers can improve the layout to gain more control over manufacturing results and yield. In LFD, the goal is to make a design so robust that it is much less sensitive to process window variations.

LFD relies on “process kit” information, encompassing RET recipes, process models and parameterizable rules to be checked. With this kit, designers can run simulations to see how their layout will print under a particular lithographic process window. The simulation results can even include recommendations about areas in which modifications would be most likely to improve yield. Designers can then make modifications to the layout in their native layout design environment. Previously, most of yield control was in manufacturers' hands; with an LFD methodology, much of the responsibility for yield control is in designers' hands.

At first glance, an LFD flow may sound overwhelming for designers. Very few, if any, chip designers have lithographic knowledge or experience. For this reason, LFD data must be presented in a manner that can be easily incorporated into the designer's layout and flow. Ideally for designers, the litho-friendly design tool will plug into their flow much like an iterative design step, using the same layout editor they use for the initial design. The process kit, not the designer, should be aware of the details pertaining to pattern transfer at the foundry, including OPC. Simulation information will be presented to the designer much in the way DRC rules are presented now. The goal of achieving a “DRC clean” design will transform into a goal of achieving a “DRC and LFD clean” design.

As designers become used to working in LFD mode, they will learn what design elements will respond favorably to manufacturing processes. In time, users will be designing in preventive mode; that is, naturally practicing manufacturing process-aware design. And on the foundry side, yield managers will be able to minimize OPC and masks will be easier to make.

Capturing process variability to improve layout robustness is a major new step in DFM. With the work being done today, a foundation is being established for managing the impact of yield inhibitors with each new process node.

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