Calibre nmOPC

Next Generation Platform for Computation Lithography

Product Launch - Editor Presentation

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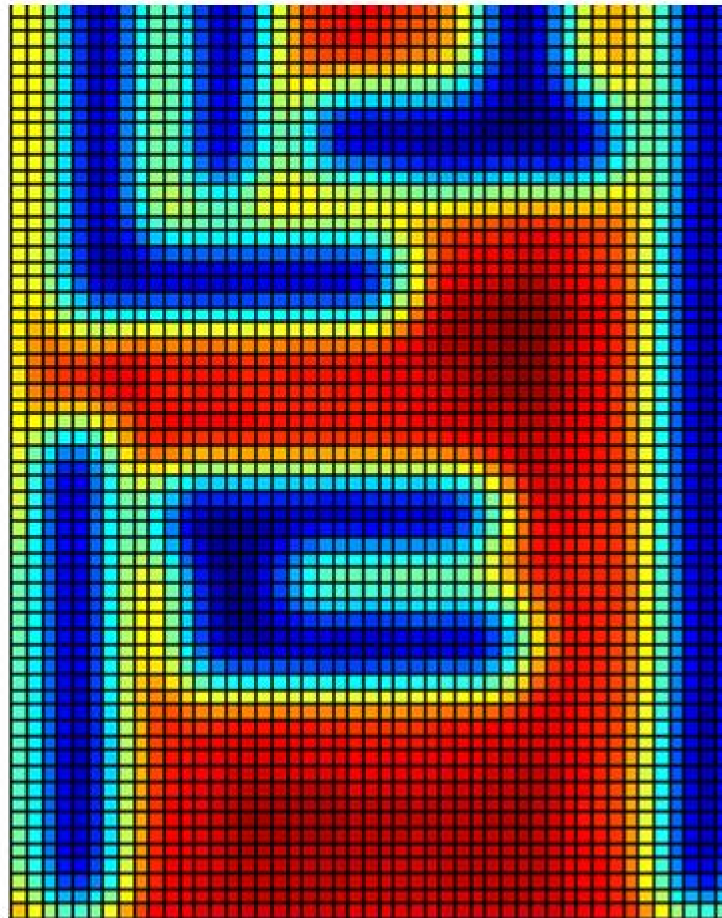
VP AND GENERAL MANAGER
DESIGN TO SILICON DIVISION

November 29, 2006

Mentor Graphics®

Introducing Calibre nmOPC
Accelerating Customer Success at 45nm



Key Product Capabilities

- **Grid-based, Dense Simulation Engine used for OPC**
  - First introduced by Mentor in Calibre OPCverify
- **Co-Processor Acceleration Capability**
- **New Streamlined Hierarchy Engine**
- **4th Generation Modeling**
- **Design Intent Awareness**
  - Preserves Functionality
- **Process window correction**

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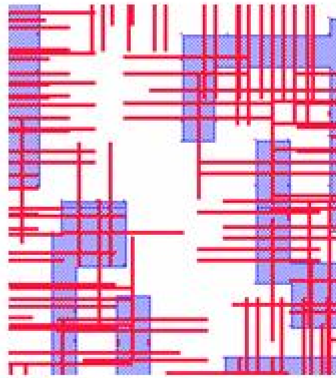
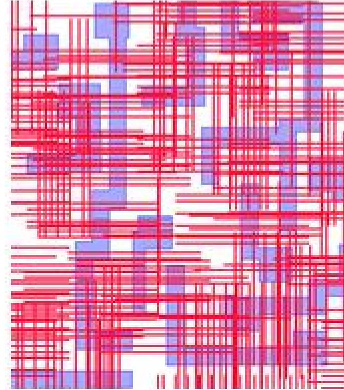
Why dense simulation?

Grid-based simulation more efficient with increasing layout density

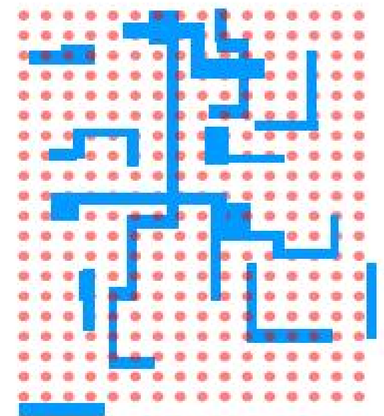
65nm sparse simulation

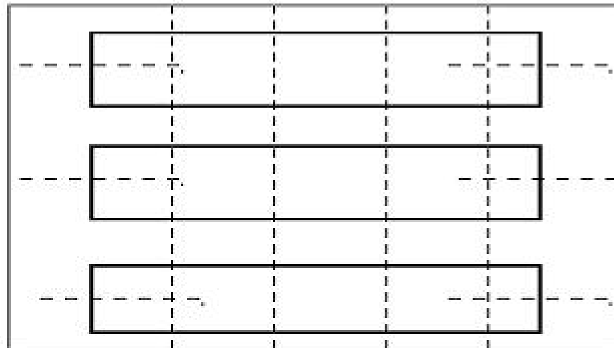


45nm sparse simulation



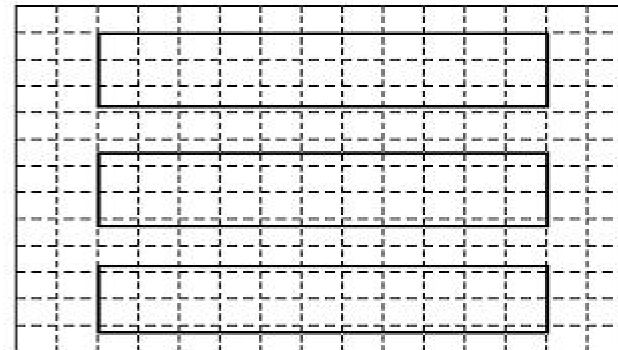
45nm dense simulation





10 Sites/Shape; 15 simulations/site; 450 simulations

OPCpro



Grid-based simulation sites; 182 simulation sites

nmOPC

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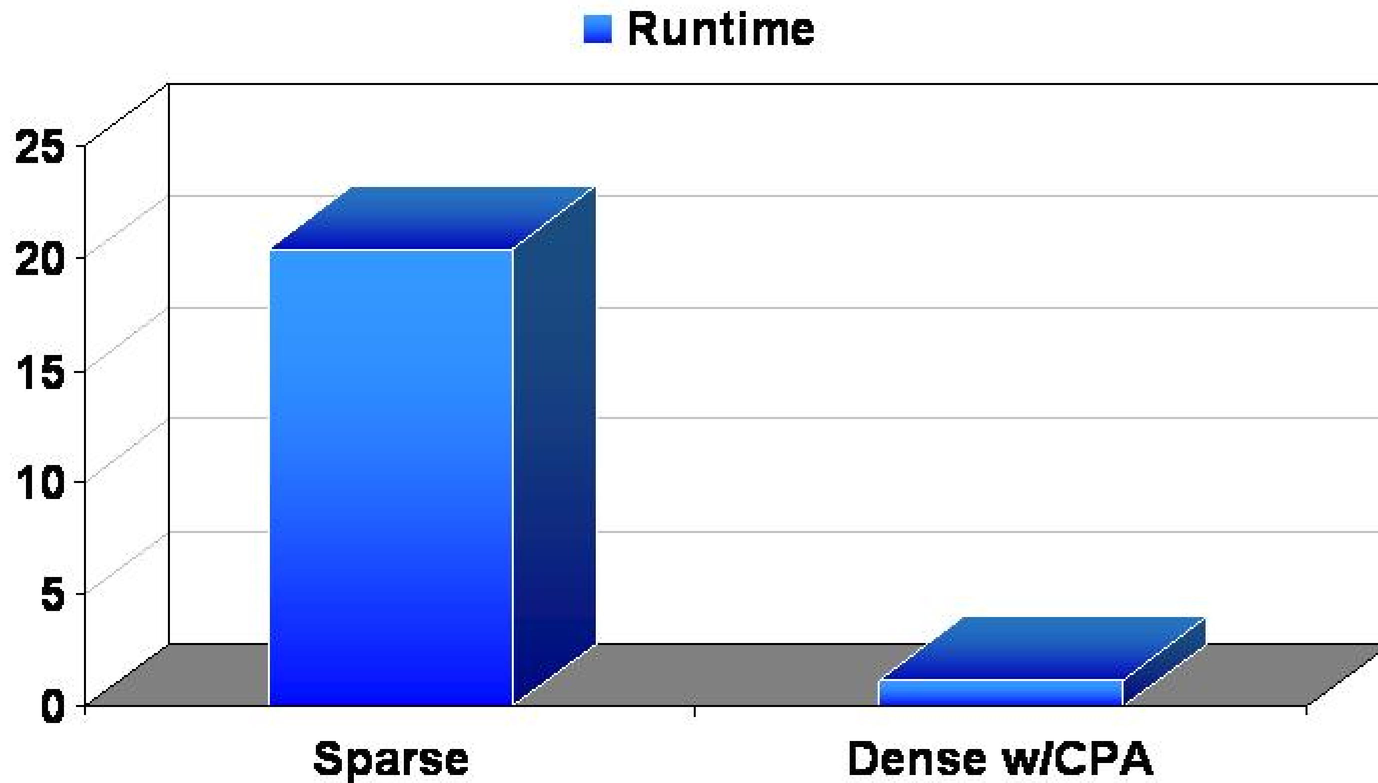
Critical Layer Runtime Advantage



45nm Poly Layer Design equivalent recipe

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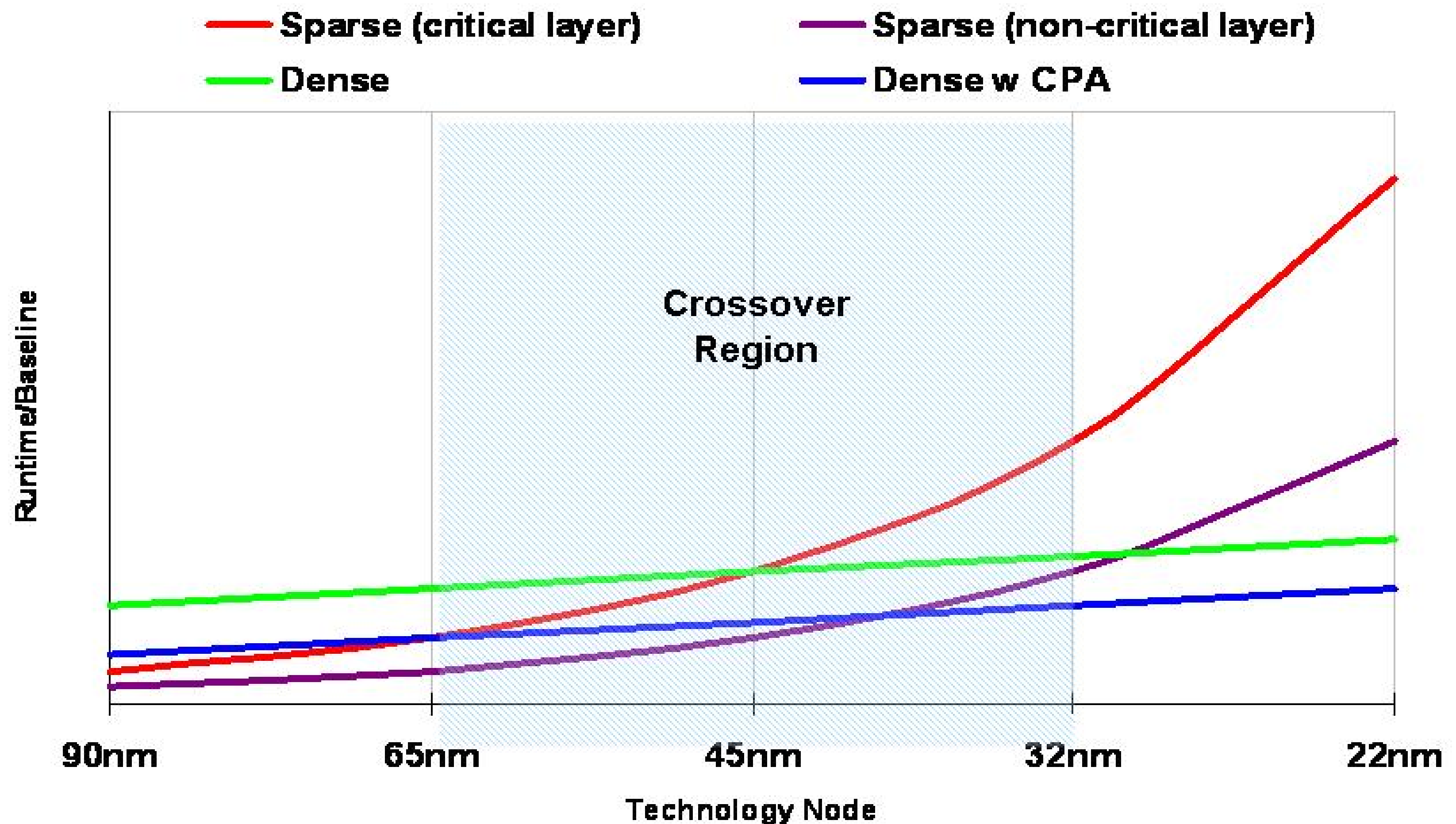
Dense Computational Efficiency vs. Sparse



- Crossover point depends on OPC Recipe and Chip Style

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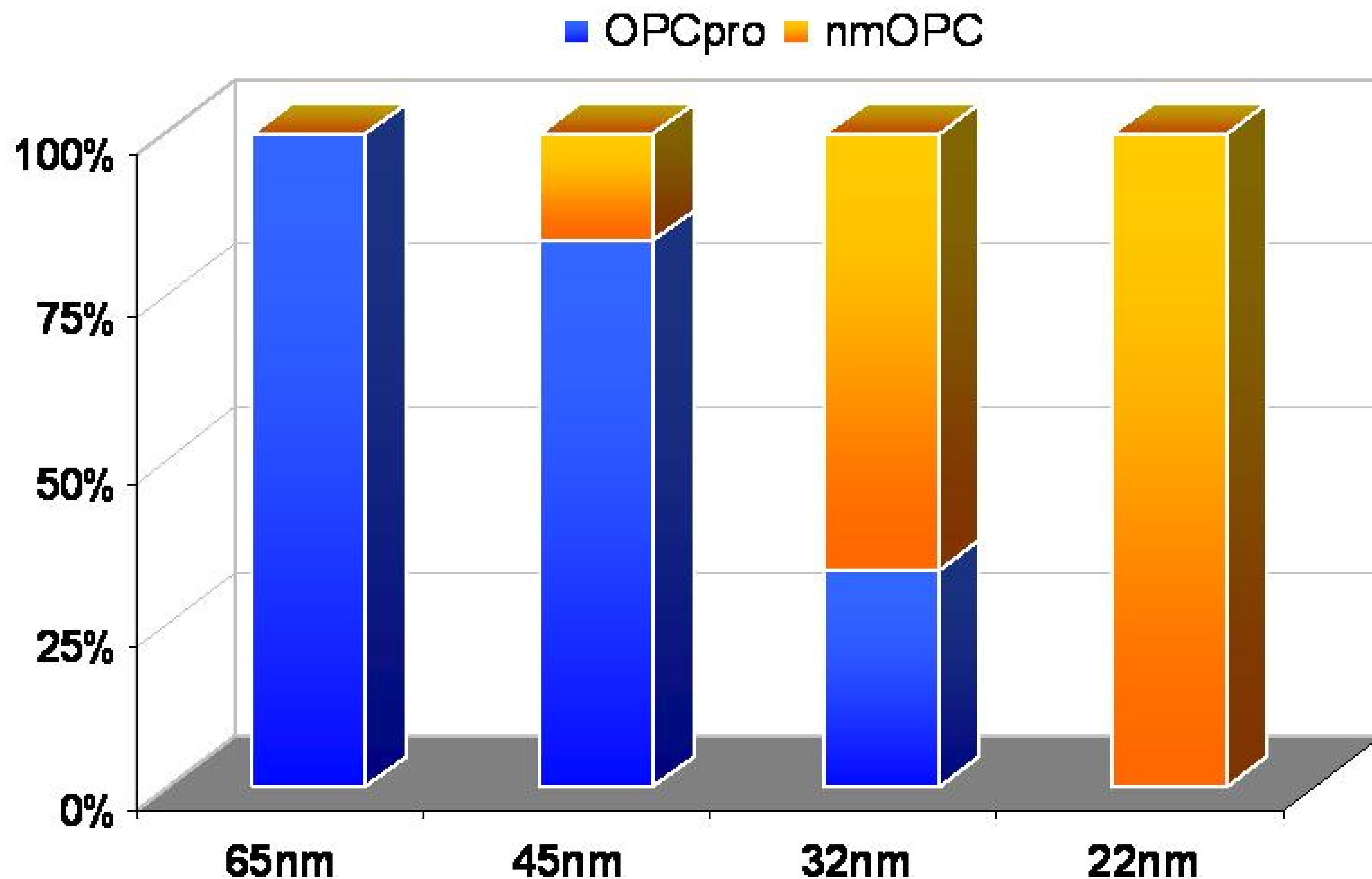
Deployment Will Utilize Both Mentor Tools



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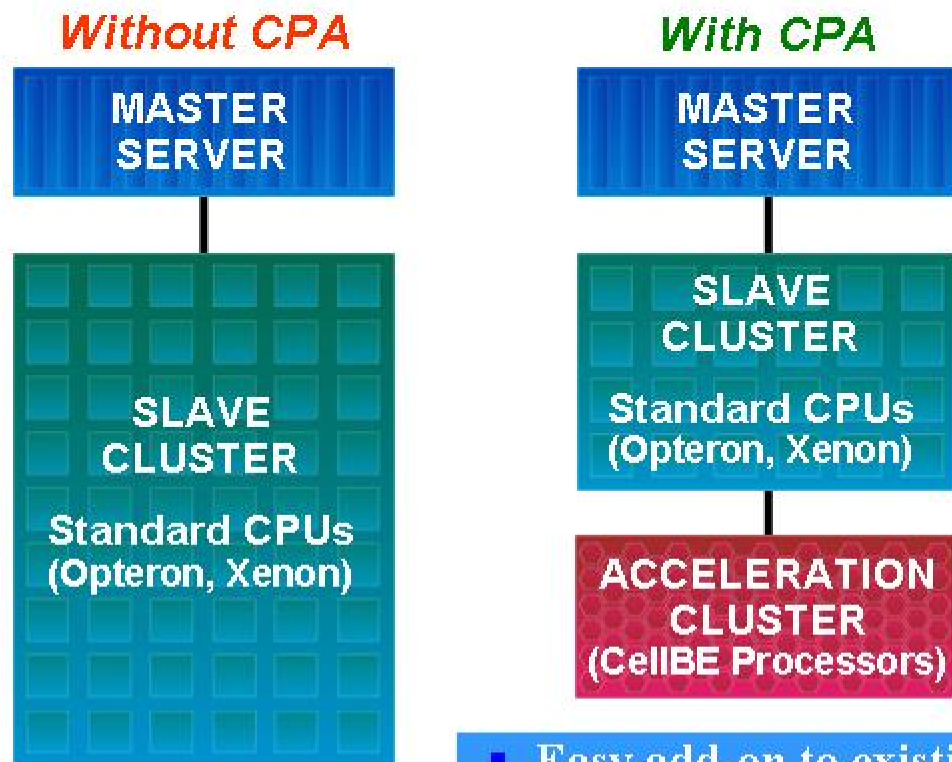
Co-Processor Acceleration (CPA)

Uses High Performance CellBE® processor for Image Simulation



- Easy add-on to existing compute cluster
- Modular – expandable
- Similar form factor as existing cluster

Note: Cell Broadband Engine is a trademark of Sony Computer Entertainment, Inc. Cell BE is a collaborative development by Sony, Toshiba and IBM.

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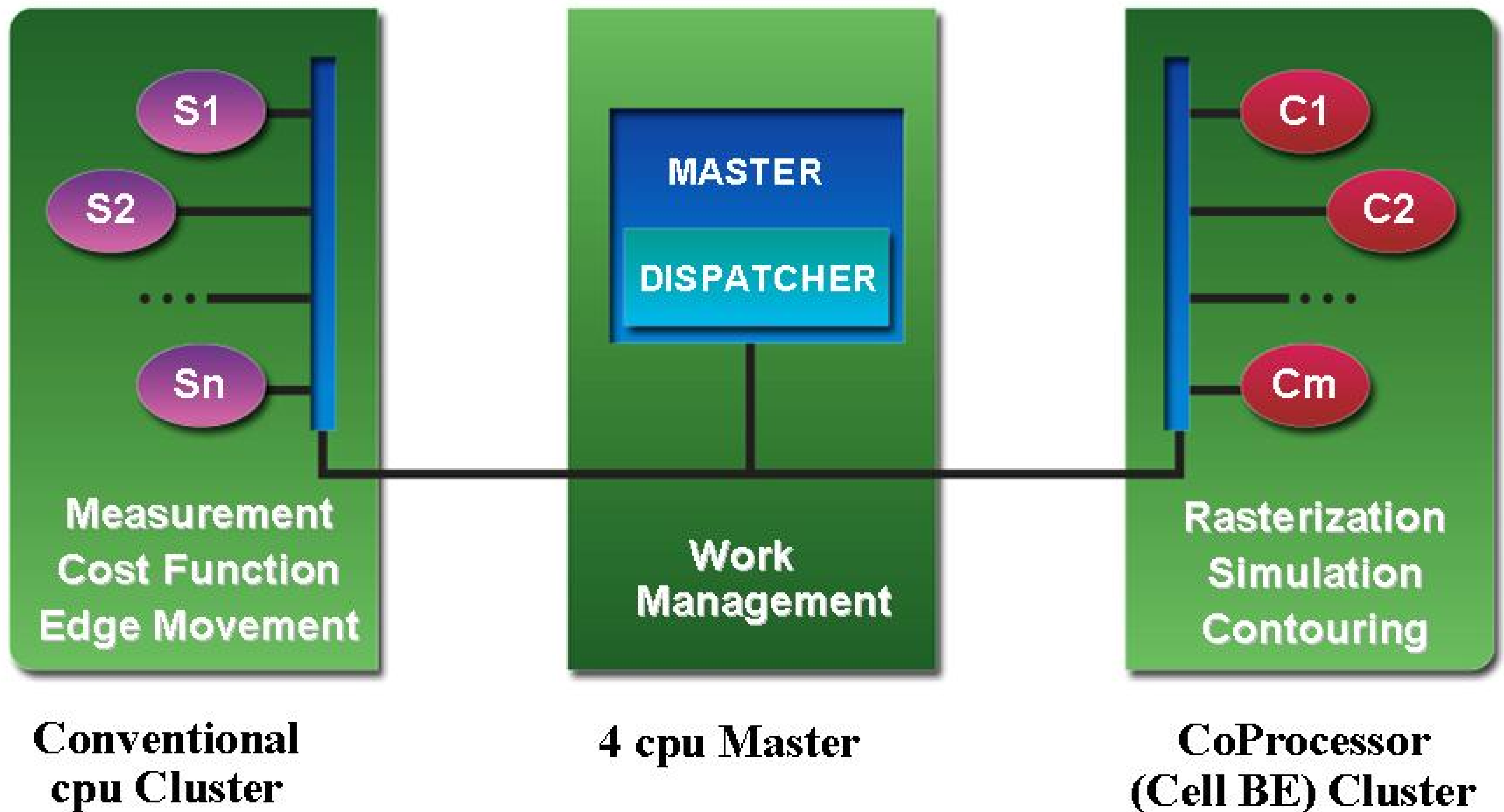
Matching the Task to the Architecture



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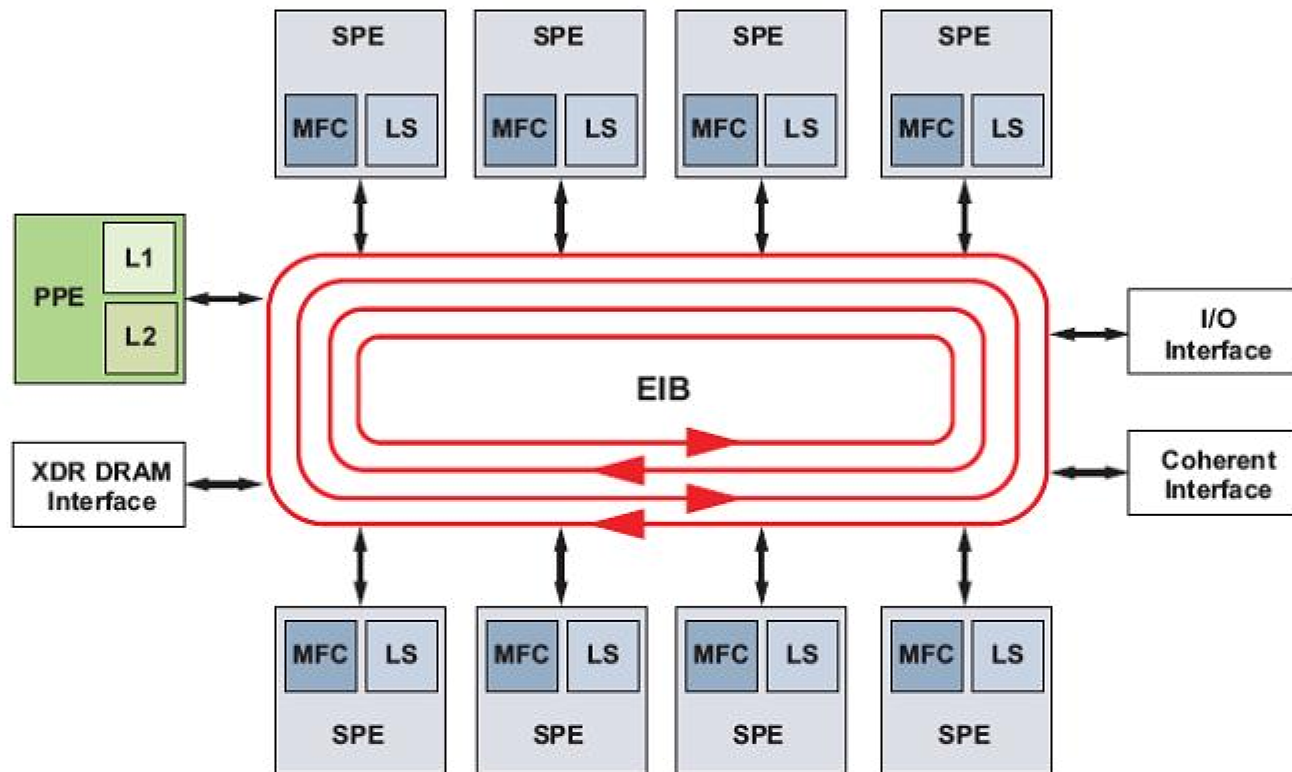
Why Cell BE?



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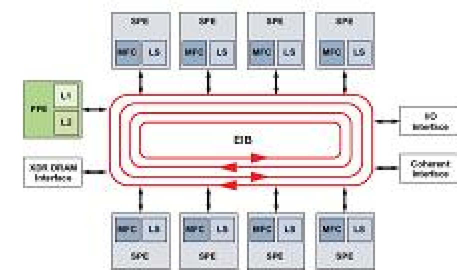
Why Cell BE?



- Supercomputer on a chip; network on a chip
  - 1 Power PC + 8 Synergistic Processing Elements
  - Unique architecture for image processing
- Standard Hardware Platform
- > 7X more computational power (GFLOPS) than FPGA's
- Software programmable for rapid implementation
- Calibre OPC simulations using FFT's are ideally suited for this processing platform
  - > 80% OPC run time consumed in simulation
  - 50 to 100x acceleration of simulation component of OPC

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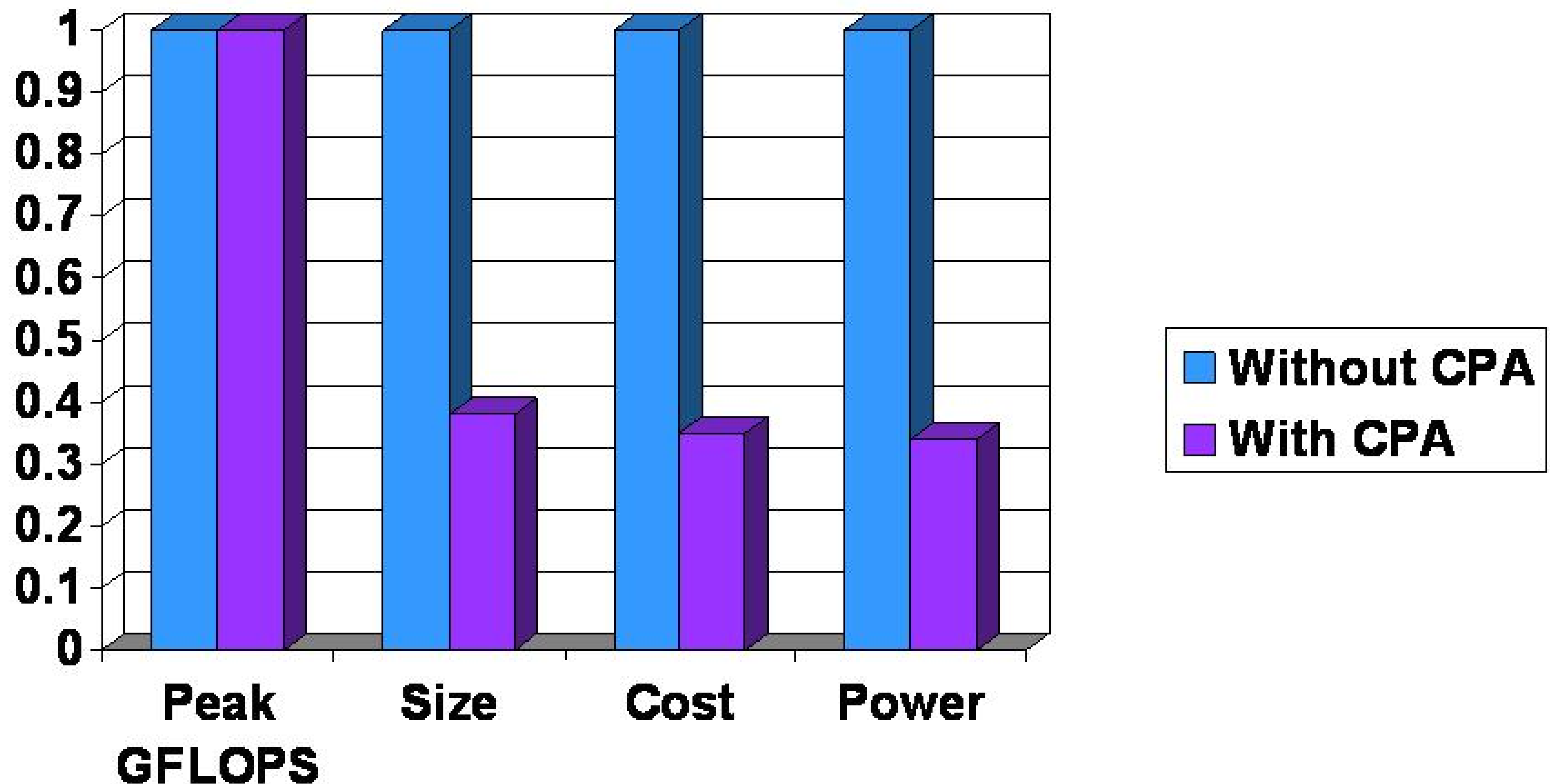
COO for a High Performance Cluster

(with and without co-processor acceleration)



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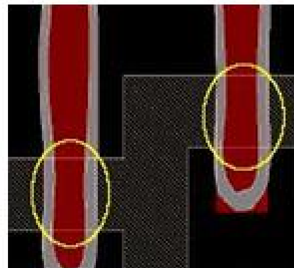
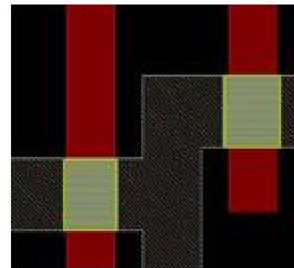
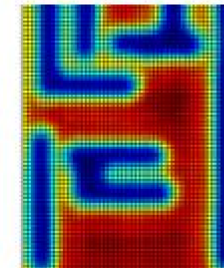
The Culmination of a Very Busy Year

JAN	FEB	MAR	APR	MAY	JUN	JUL	AUG	SEP	OCT	NOV	DEC

January 9	March 6	July 10	November 29
			
Calibre OPCverify	Calibre LFD	Calibre nmDRC	Calibre nmOPC

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The Rise to Power…of Power *

- *"Although energy costs account for less than 10% of most IT budgets, they could rise to more than 50% in a few years."* Gartner

45nm without CPA

- **Computing Capacity**

- 750 to 1000 cpus

- **Power Requirements**

15 - 20 kw / rack + Cooling

45nm with nmOPC

- **Computing Capacity**

- 100-200 cpus + 1 CPA cluster (25-50 cell processors)

- **Power Requirements**

$75-100k energy savings/ year / system

* Jerald Murphy, Robert Frances Group

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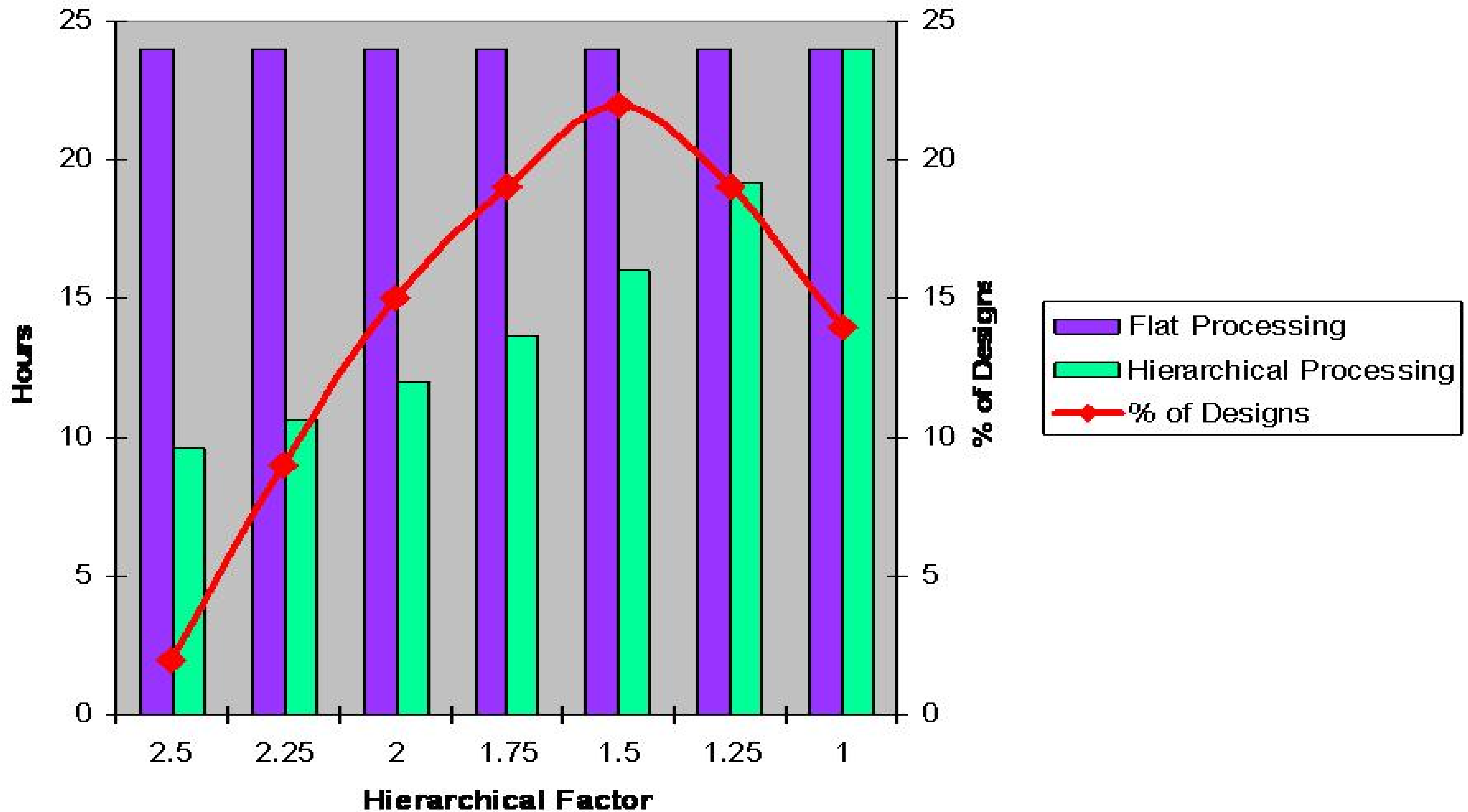
New Streamlined Hierarchical Processing

Accelerates Runtime to Improve COO



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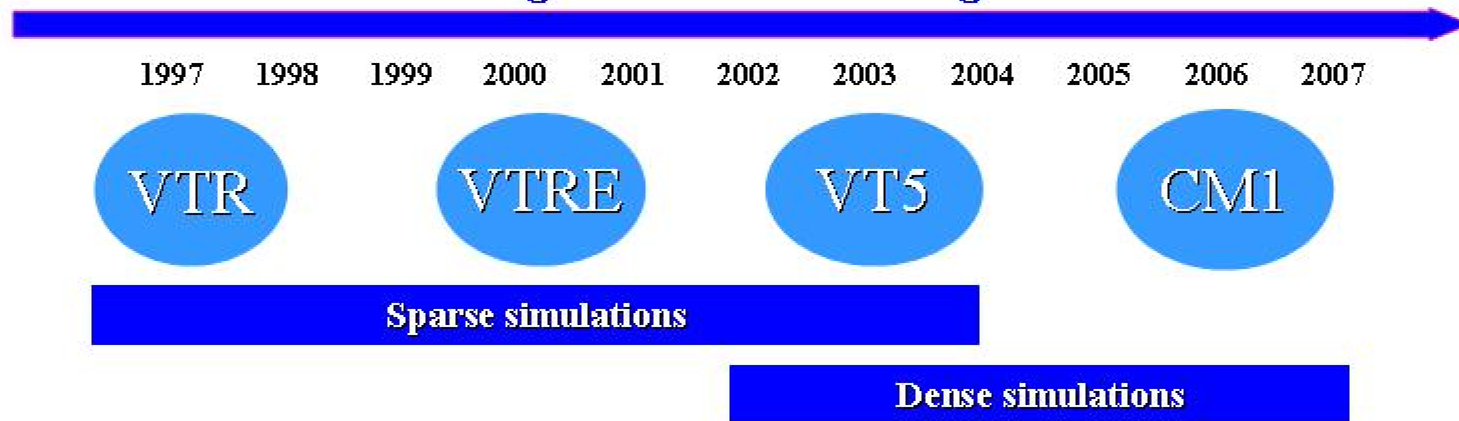
Dense Simulation Resist Modeling



	VT5	CM1
Accuracy	+	++
Dense Simulation Speed	+	++
Stability	+	++
Calibration Automation	+	++
Process Window Accuracy	+	++

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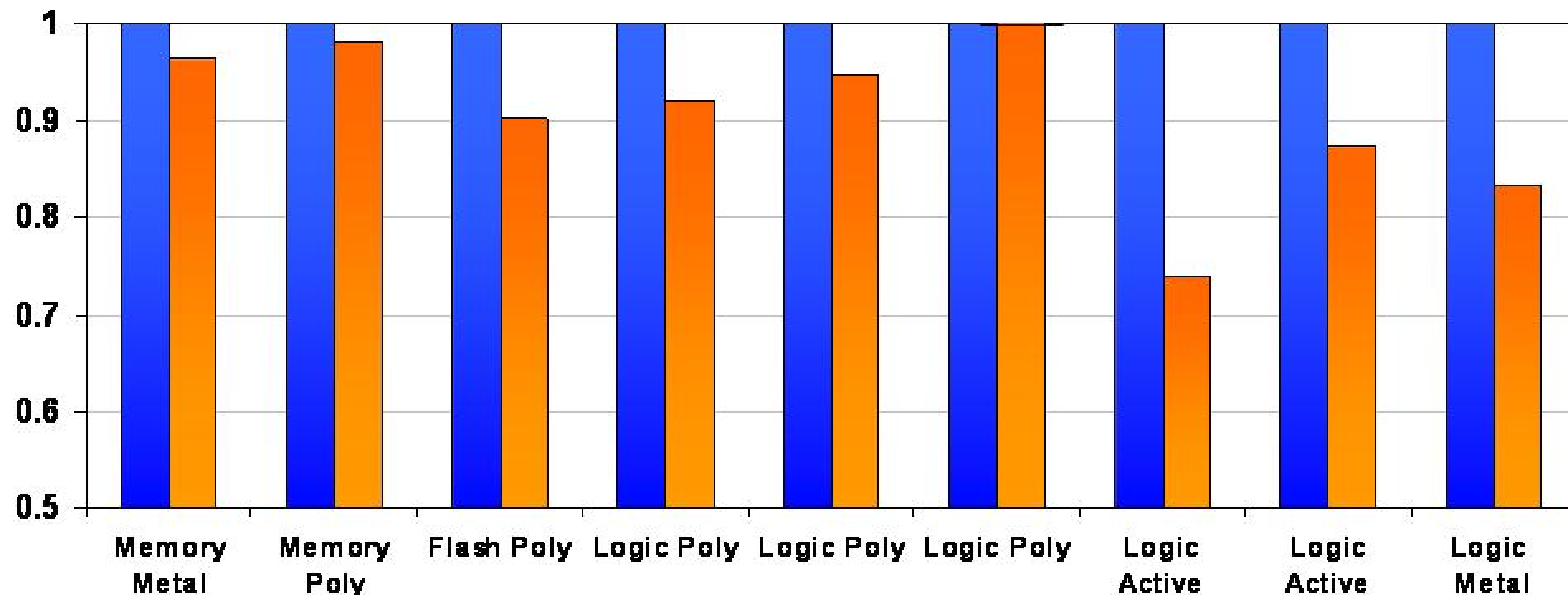
4th Generation Resist Process Modeling

Accurate, Stable with Automated Optimization



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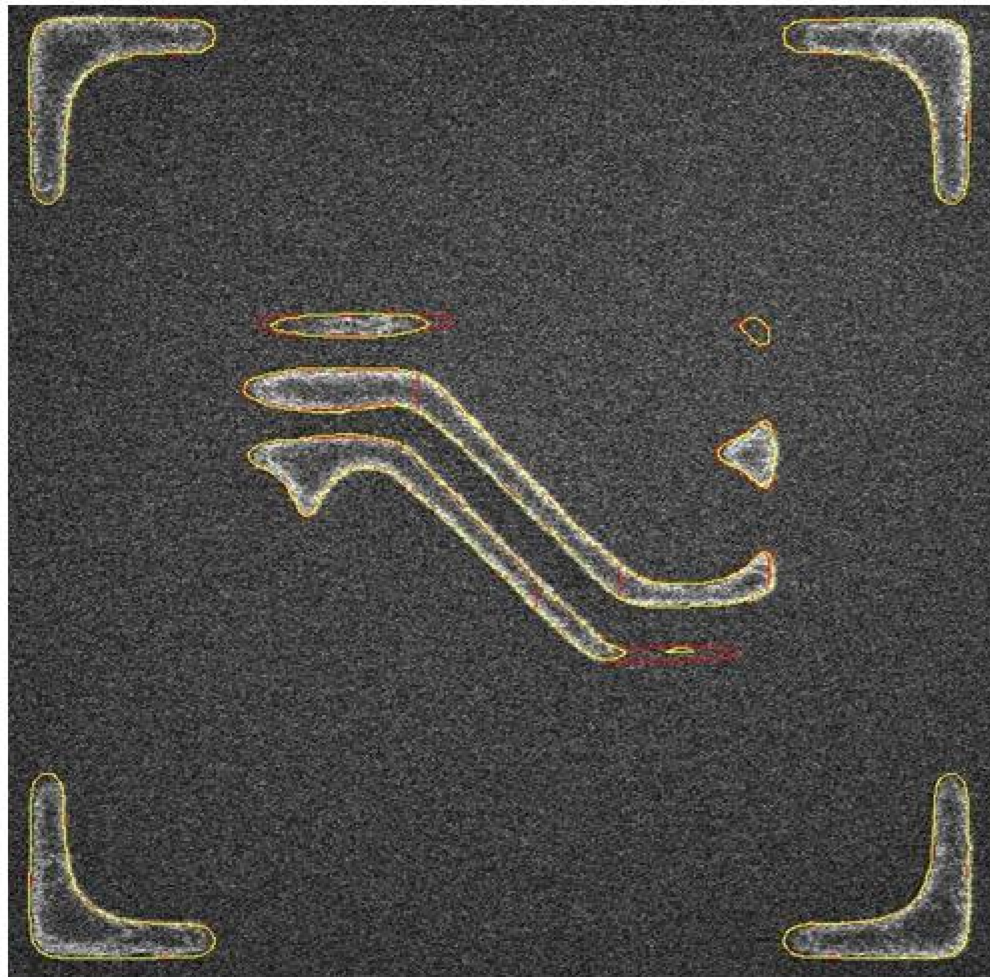
CM1 – VT5 Process Window Accuracy Comparison



Yellow VT5
Red CM1

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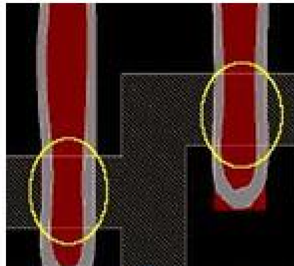
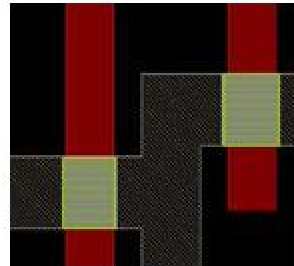
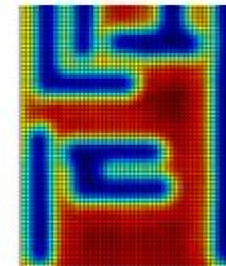
Unified Infrastructure Across the Product Line







Calibre OPCverify

Calibre LFD

Calibre nmOPC

CM1 Modeling

Dense Simulation

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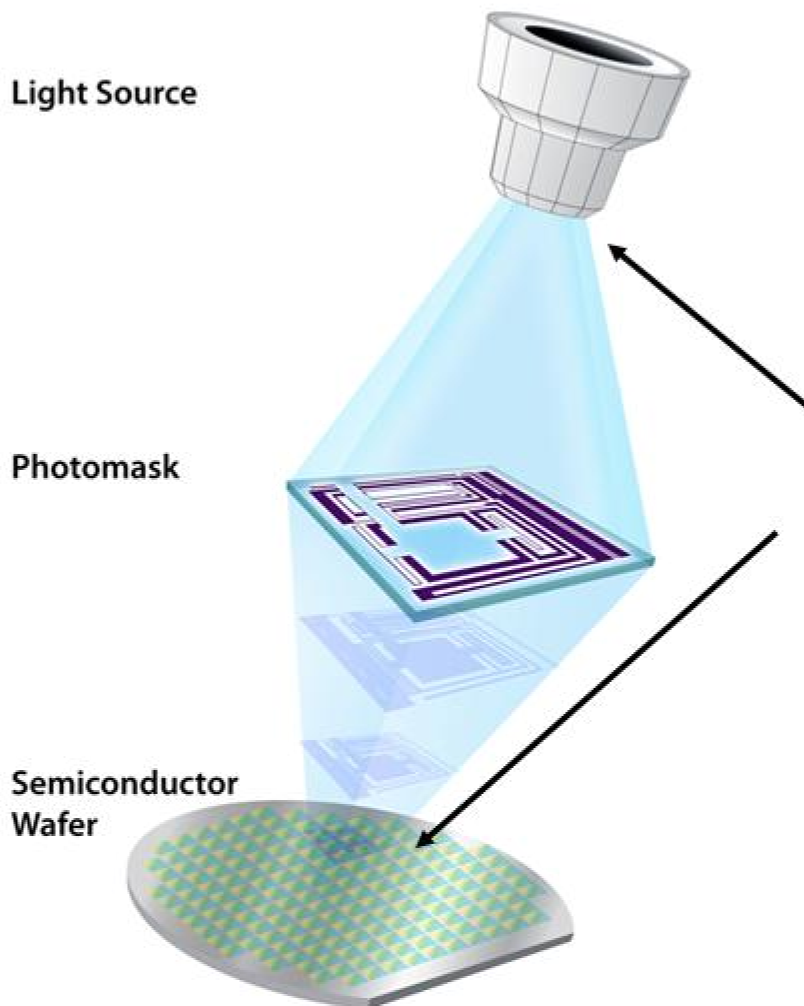
Sources of Lithographic Variability



Two main sources of lithographic variability

- Dose: variation in intensity
- Focus: variation of wafer in z axis

Defines a manufacturing window, commonly referred to as "the process window"

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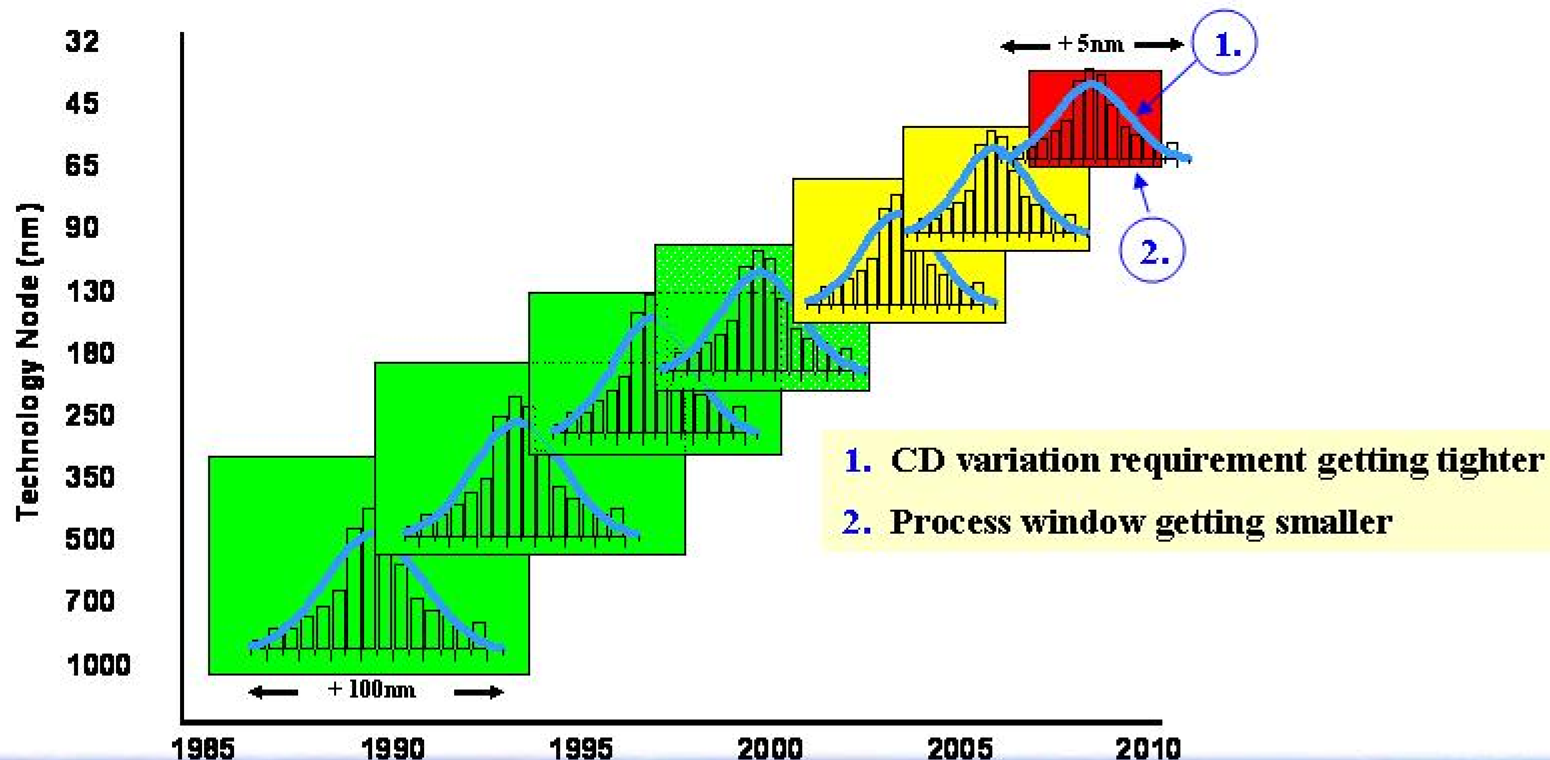
Image Resolution Highly Sensitive to Process Window and RET Strategy

- Increasing sensitivity of pattern fidelity to process variation and layout topology
- Process Window OPC checks required to assure yield ⇨ more computation, more time



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Process Window OPC

- **Define a Process Window (in this case, +-1nm mask, +-10% dose, nominal + defocus)**
- **Use OPC to <u>decrease</u> sensitivity to: Dose, Focus, Mask Sizing**

PW Failure with acceptable nominal condition OPC

Optimized OPC correction to prevent PW failure

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Design Intent: Contact Overlap

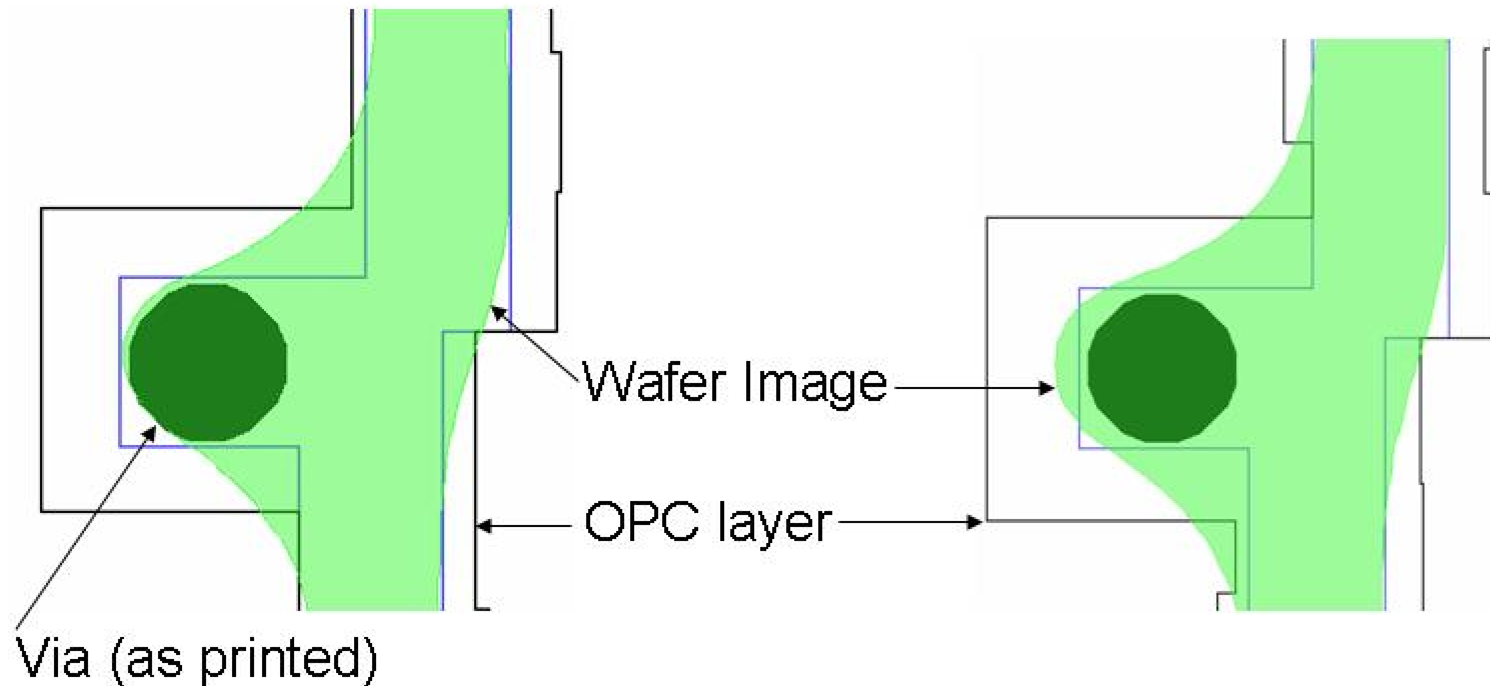
nmOPC ensures adequate contact coverage

Ordinary OPC

- Optimizes edge placement error for correction layer

Circuit-aware OPC

- OPC prioritizes contact coverage over edge placement error
- Improved process yield



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Calibre nmOPC Product Introduction

- **Addresses critical technical and business issues in Computational Lithography for the 45nm process node**
  - **Computational Complexity – supercomputer capacity required**
  - **Turn Around Time (TAT) - must not increase over 65nm**
  - **Cost of Ownership - geometrically increasing**
- **Next Generation OPC tool from the leader in model-based OPC tool deployment with 32 fabs using Calibre OPCpro**
- **Developed within Mentor by the same architects that created Calibre OPCpro**
  - **> 150 years of OPC experience represented in this development**
  - **Collaborative development support from 6 key IC manufacturers**

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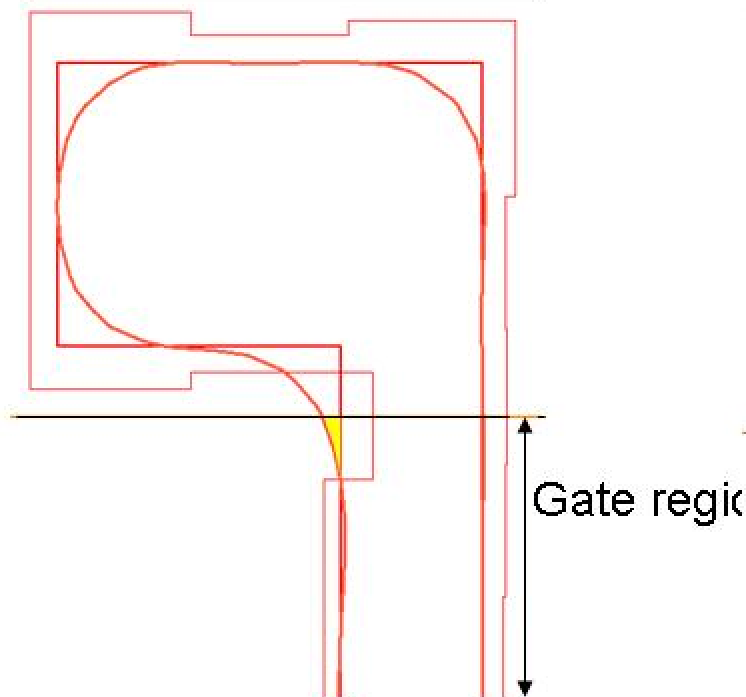
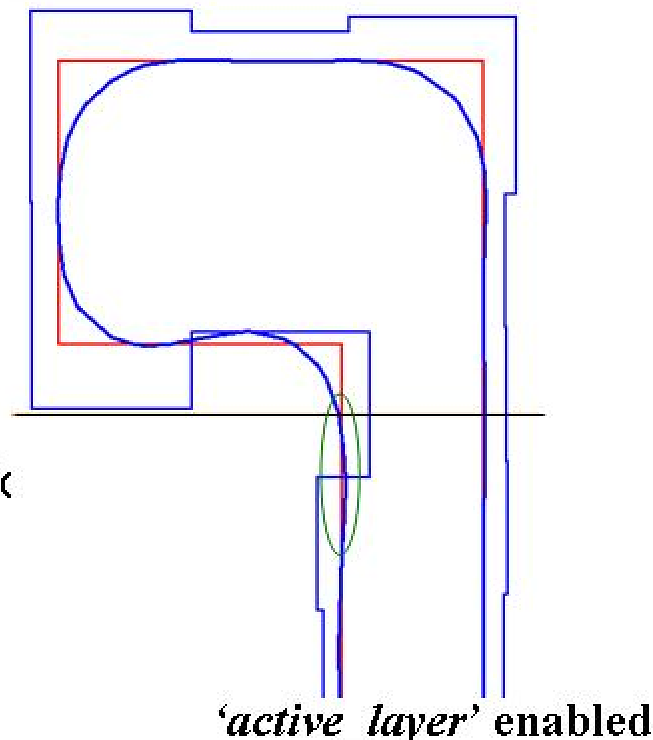
Gate CD Prioritization





- Single command in nmOPC optimizes correction for Gate CD uniformity
- Simplifies set up file generation
- Improves parametric yield

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Meeting the Challenge of 45nm and Bellow

- Solves the crisis in cost of ownership and turn around time
- Provides the new level of accuracy required for low k1 imaging
- Add new yield-enhancing functions that ensure image fidelity across the process window targeting design intent

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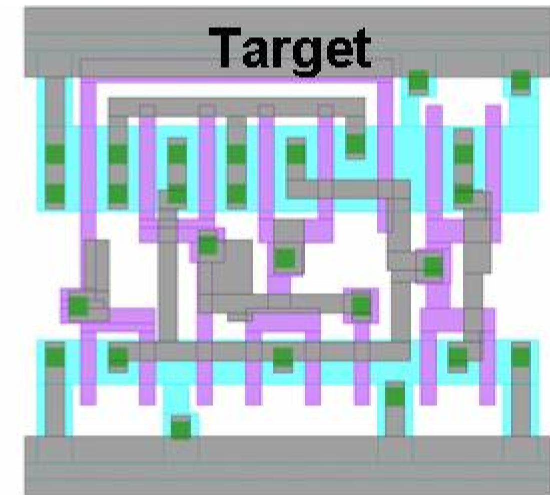
Mentor Graphics®
1981-2006
25 Years of Innovation

Increasing Difficulty of Low K1 Imaging

10
1
0.1
ABOVE WAVELENGTH
SUB WAVELENGTH
3.0 µm
2.0 µm
FEATURE SIZE
1.0 µm
0.6 µm
436 nm
365 nm
LITHOGRAPHY WAVELENGTH
0.35 µm
0.25 µm
180 nm
248 nm
193 nm
130 nm
65 nm
45 nm
1980 1985 1990 1995 2000 2005 2008



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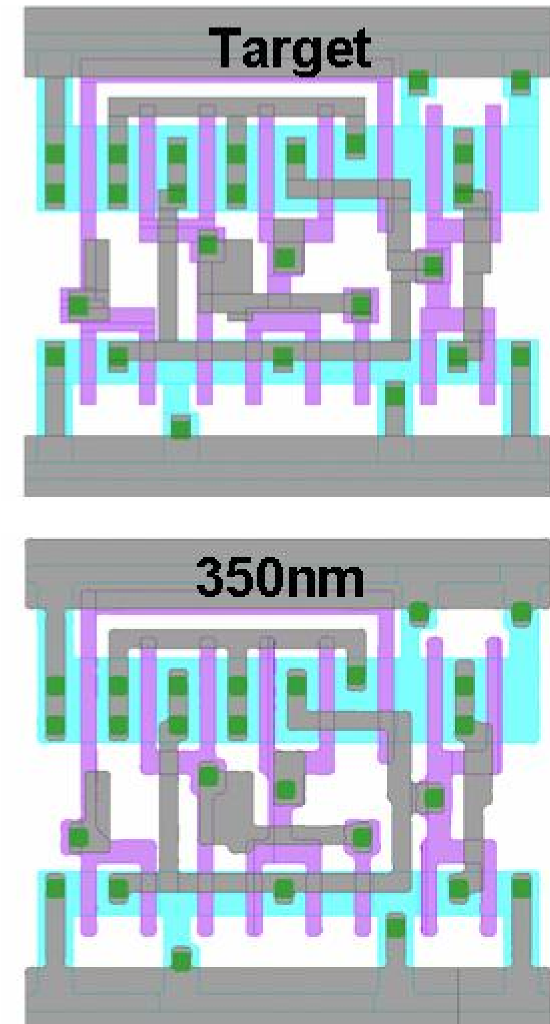

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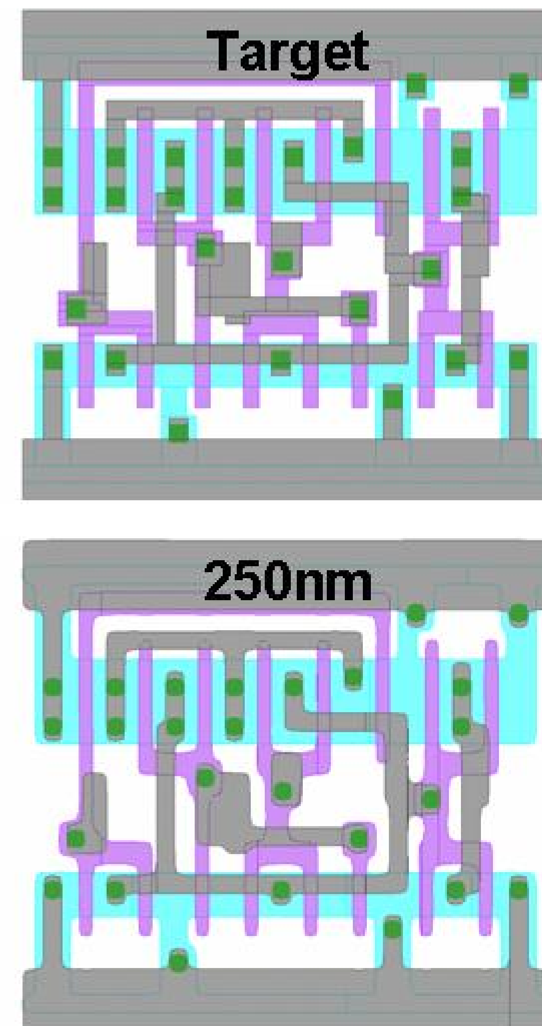

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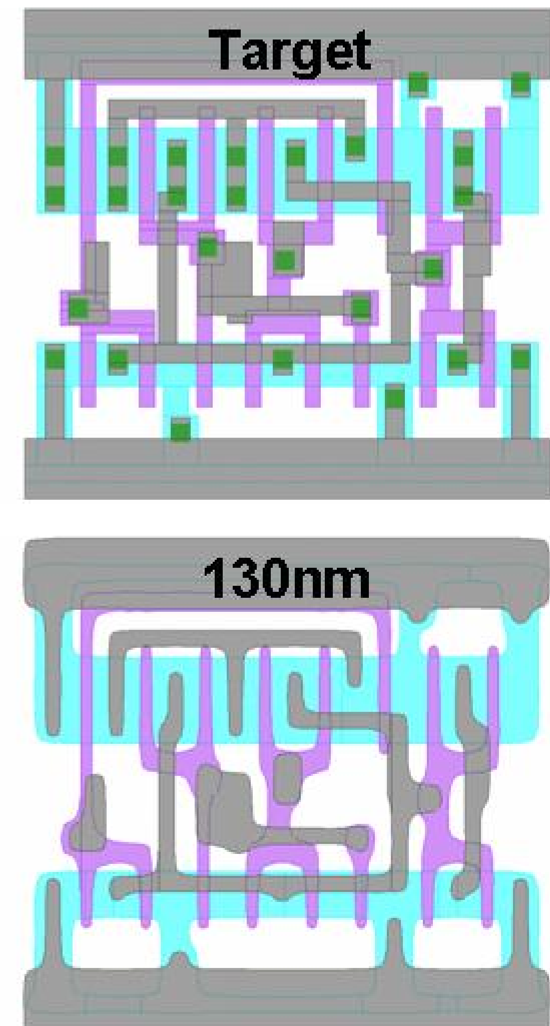

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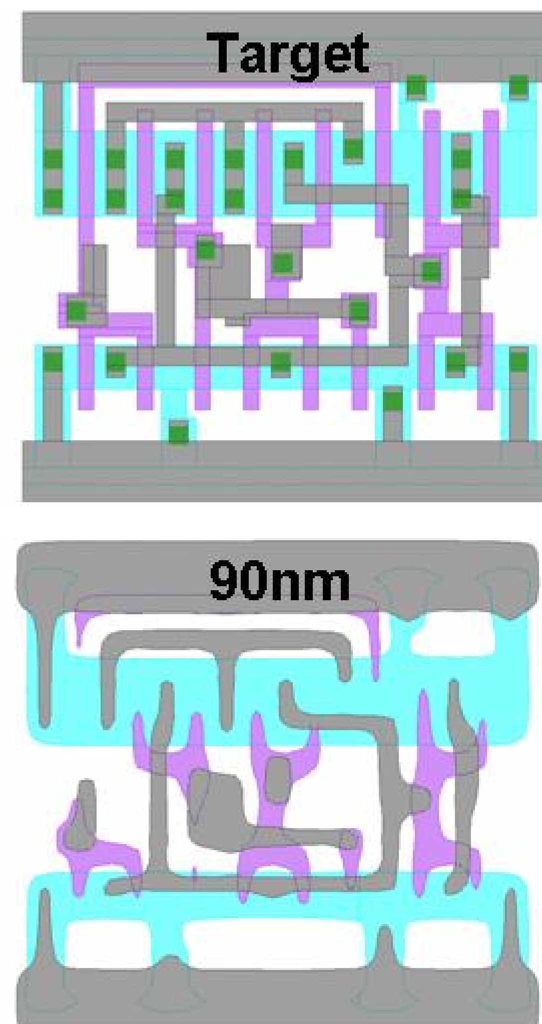

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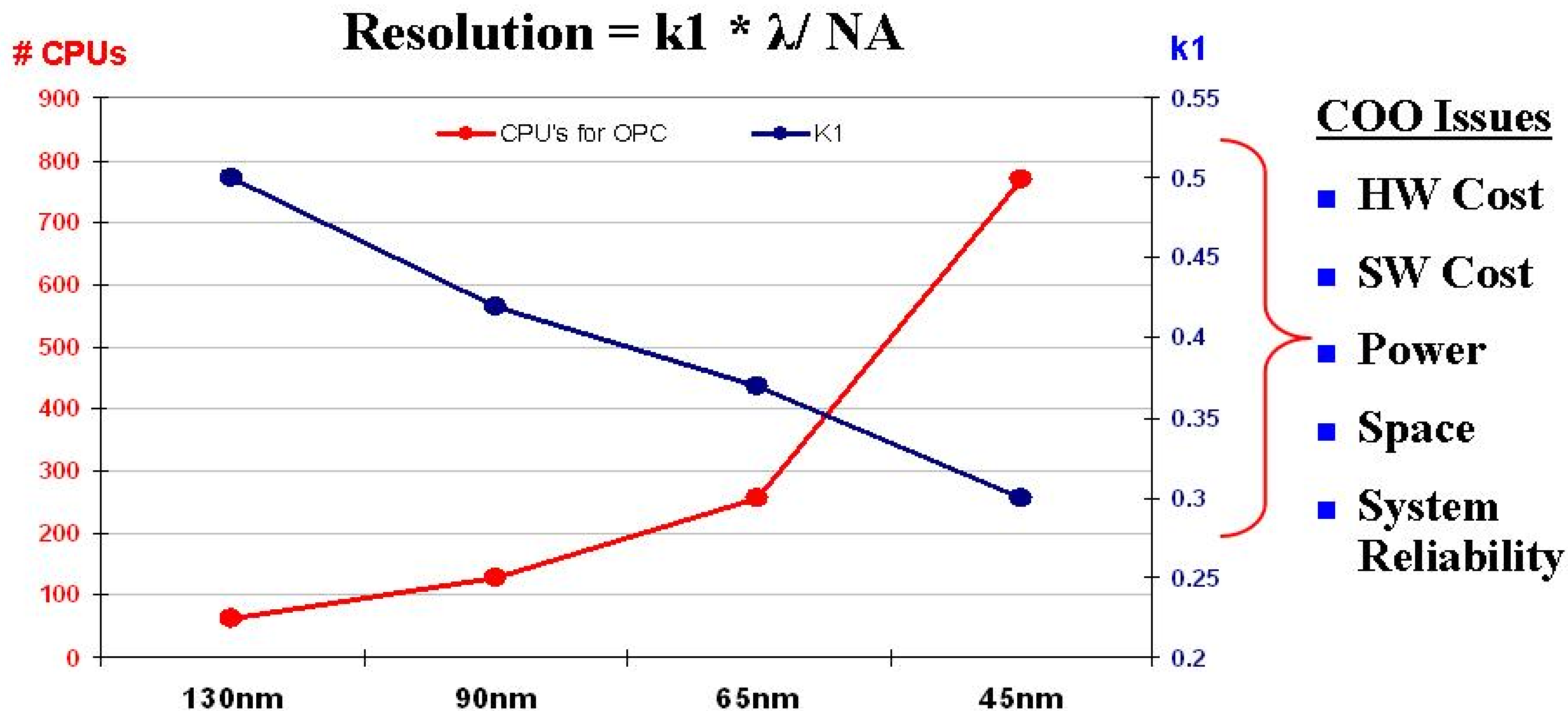
Computational Complexity at 45nm Creates a Compelling Business Need



- More complex models – more simulation time required
- Dense design layers: more shapes being processed

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