

Figure 1A – Using the Topology Planner, an engineer can define, analyze and capture bus path structures.

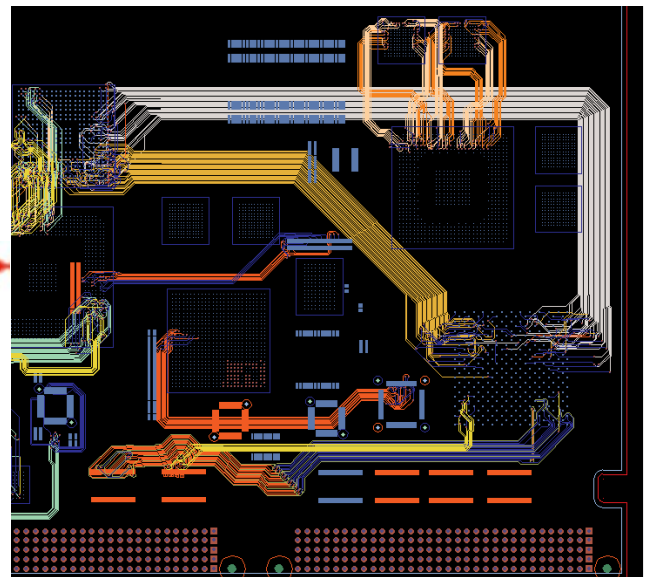


Figure 1B – The Topology Router then can auto-route the buses following the plan.

## Introduction

Over the years, designers implementing dense boards have largely ignored the use of autorouters for the simple reason that they cannot route with the intelligence of an experienced designer. The basic problem is that while an engineer or designer sees the problem at a higher level and can visualize the flow of busses and interconnects between components, an autorouter attacks the problem one interconnect at a time. The results of this auto-routing may be electrically correct but lack in manufacturability, density and ease of change to say nothing of esthetic form.

When planning a dense printed circuit board, engineers typically sketch the physical bus systems and sub-system architecture on paper, which then serves as a guide for the board designer to manually follow. Typically, the designer has a vision of component placement and interconnection flow that is crucial during early planning, but translating this into something an autorouter can understand is next to impossible. Therefore, a designer must weigh competing forces, such as design complexity and project timescales, before commencing the project. Invariably the designer often sacrifices the huge time savings autorouters could provide and instead relies solely on manual routing techniques to complete the design.

To combine the knowledge of an engineer, the skill of a board designer and the power of an autorouter, Mentor Graphics has developed a powerful topology planning and routing technology. This technology provides automated planning tools for the engineer and designer to evaluate and plan bus-system interconnects early in the design phase. The topology plan is stored with the layout design database and is used to guide the topology-router and produce high quality results that mimic the manual routing of a designer in a fraction of the time.

## Major product benefits:

- Easy-to-use bus planning for the engineer
- Digital communication of plan to the designer
- Auto-routing of buses following plan
- Automated controls for delay tuning, shielding and other constraints
- Plan saved with design database for iterations and design re-use

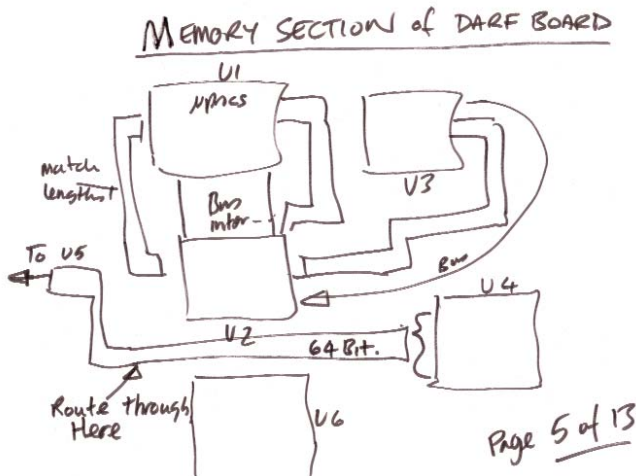


Figure 2: In the past, engineers sketched bus structures on paper:

### Planning Drives Auto-routing

In the past, an engineer would sketch out the bus structures (Figure 2) on a piece of paper then pass this to the designer. This process was lengthy and error prone. Using the paper method, the engineer had no way to understand if the proposed layout met high-speed delay constraints or if it is possible to connect the components in the given placement on the target number of layers.

Now, with the topology planner and router functionality, this process is fully automated. Figure 1A shows bus paths easily defined in the topology planner that guides the autorouter. Each bus contains information about the signals (bits), clearances and branch points as well as the routing layer and topology rules the autorouter must obey. This plan

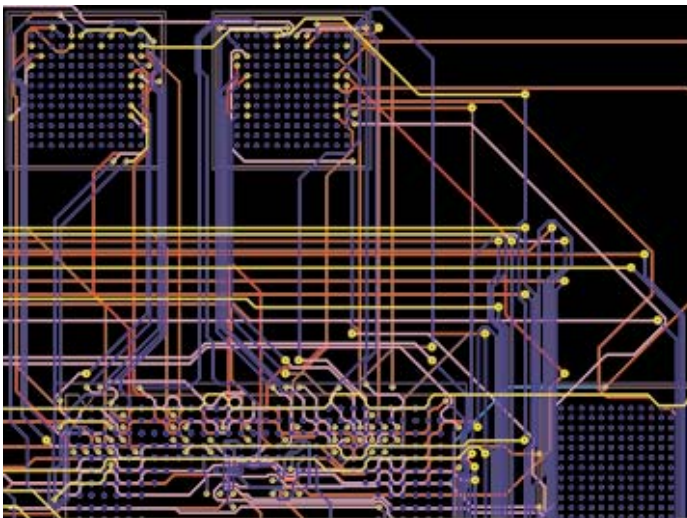


Figure 3: Auto-routers typically route one connection at a time without recognition of bus structures.

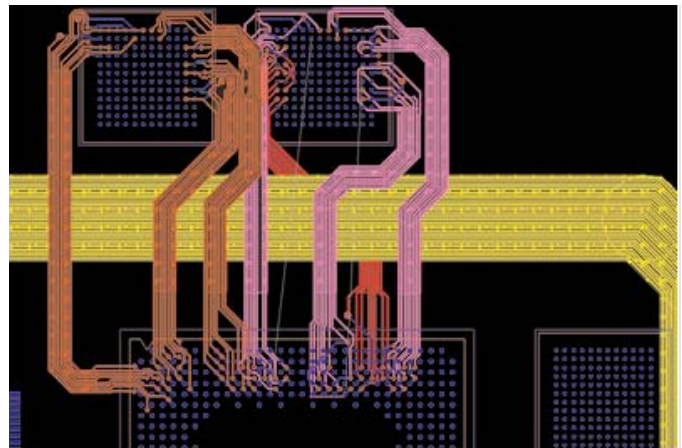


Figure 4: Autorouter follows the bus structure plan.

can be developed by the engineer assuring the buses will meet delays goals thus avoiding a potential iterative process of paper bus definition, routing, delay analysis, re-definition, and re-routing by the designer.

Bus structures can include splits, branching, layer changes and connection points to many components. The autorouter follows the bus paths routing complete bus structures in and connecting to the component pins as specified.

Unlike typical bus auto-routing results, as illustrated in Figure 3, Figure 4 shows the results of the topology router following a topology plan. Using this methodology, the plan can be easily modified and additional routings performed, thus quickly and efficiently iterating to a final solution.

### Controlling the Router

During planning, the bus paths can also include additional parameters like trace shielding and via fanout preferences. Figure 5 shows a 16 bit bus making a layer change with uniform via pattern. The bus plan calls for every forth bit shielded with ground as shown with green traces. Note how the end caps of the bus are shielding on both layers as the bus changes layers. Furthermore, the shielding traces follow the bus layer transitions with their own vias. While not shown, the shielding capability also wraps around component pins and provides a frequency of vias to ground planes.

For high-speed buses that require exact matching of lengths to physical and electrical delay constraints, some areas contain tightly packed routes while other areas are set aside for tuning. Topology planning can specify where along the bus to allow tuning of delays. In Figure 6, the designer has indicated the bus path segments to allow tuning of delay.

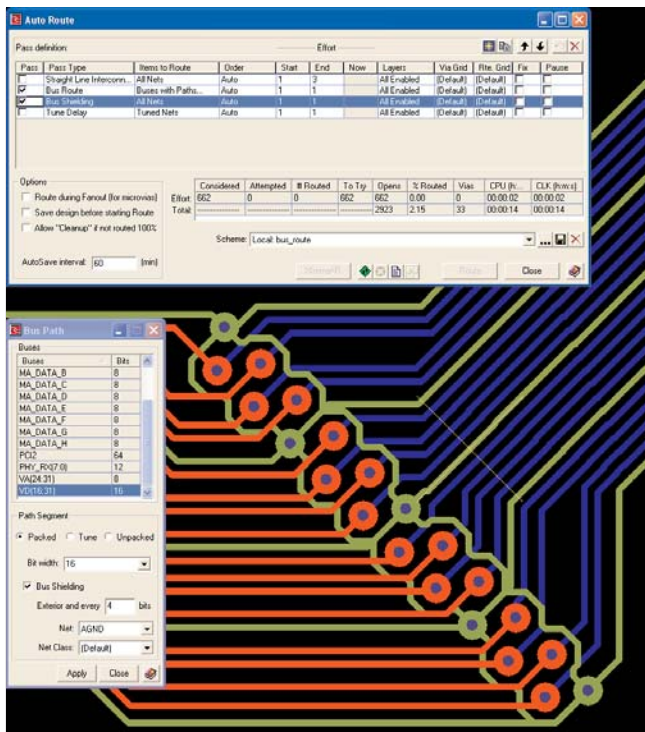


Figure 5: Trace shielding and via preferences can be specified.

While performing topology planning, designers and engineers understand that not all buses fit the model of a tightly packed path, where all bits converge into a narrow, packed structure then flow out the ends of the bus path to component pins. In the next image, there is a 64 bit bus traveling between two closely placed BGA packages. Forcing all these bits to meet into a tightly packed bus path fails so another solution is needed. Topology planning and routing offers Unpacked Bus Areas function that allows for the assignment of bus from/tos to a free drawn polygon, constrained area with specific layers and layer biasing options.

### Plan Stored in the Design Database

Engineering Change Orders (ECOs) occur frequently and at almost any time in the design cycle. When they occur during the interconnection part of the design cycle, there is a drastic impact on schedule for those PCBs that are interactively routed. With topology planning and routing, the bus paths are stored digitally with the design – whether or not

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**Corporate Headquarters**  
**Mentor Graphics Corporation**  
 8005 SW Boeckman Road  
 Wilsonville, OR 97070-7777  
 Phone: 503.685.7000  
 Fax: 503.685.1204

**Sales and Product Information**  
 Phone: 800.547.3000

**Silicon Valley**  
**Mentor Graphics Corporation**  
 1001 Ridder Park Drive  
 San Jose, California 95131 USA  
 Phone: 408.436.1500  
 Fax: 408.436.1501

**North American Support Center**  
 Phone: 800.547.4303

**Europe**  
**Mentor Graphics**  
**Deutschland GmbH**  
 Arnulfstrasse 201  
 80634 Munich  
 Germany  
 Phone: +49.89.57096.0  
 Fax: +49.89.57096.400

**Pacific Rim**  
**Mentor Graphics (Taiwan)**  
 Room 1603, 16F  
 International Trade Building  
 No. 333, Section 1, Keelung Road  
 Taipei, Taiwan, ROC  
 Phone: 886.2.87252000  
 Fax: 886.2.27576027

**Japan**  
**Mentor Graphics Japan Co., Ltd.**  
 Gotoyama Hills  
 7-35, Kita-Shinagawa 4-chome  
 Shinagawa-Ku, Tokyo 140  
 Japan  
 Phone: 81.3.5488.3033  
 Fax: 81.3.5488.3021

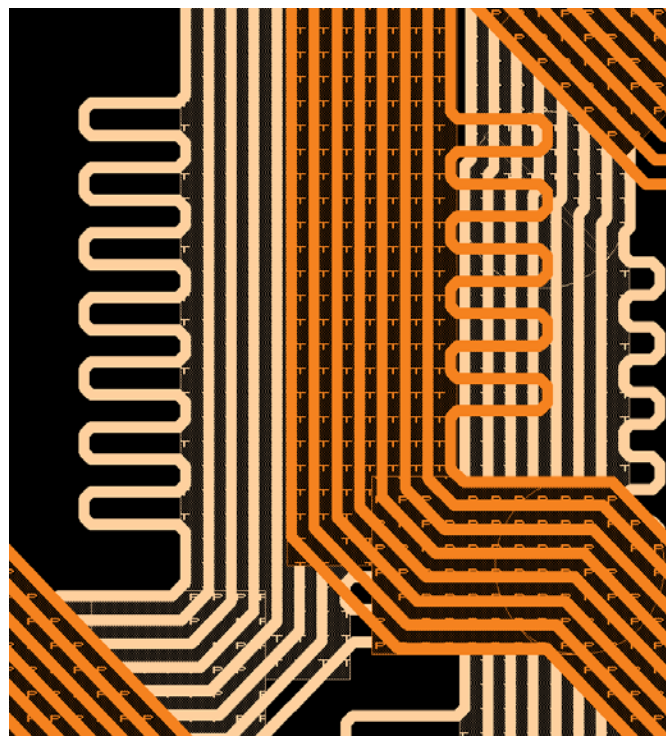
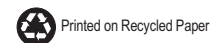


Figure 6: Areas can be defined for delay tuning.

they are routed. The topology planning tools provide more efficient ECO management allowing bus paths to be easily modified and re-routed, yet maintaining consistent results. Not only does this technology enable design changes to be performed without risking project schedules but it also reduces time-to-market through highly controlled automatic routing tools.

### The Intelligence of a Human, the Speed of Auto-routing

Mentor's topology planning and routing technology provides a unique way for the engineer, designer and autorouter to work together in planning and designing complex bus systems and avoiding the sketchpad instructions and hand-routed boards. It also compliments the designer's vision of logic flow while making ECO's easier to manage as bus paths can be quickly moved and re-routed while still maintaining design integrity. High quality/manufacturability routing is the result with reduced design cycle time.